Fundamentals of Electrical and Electronic Engineering

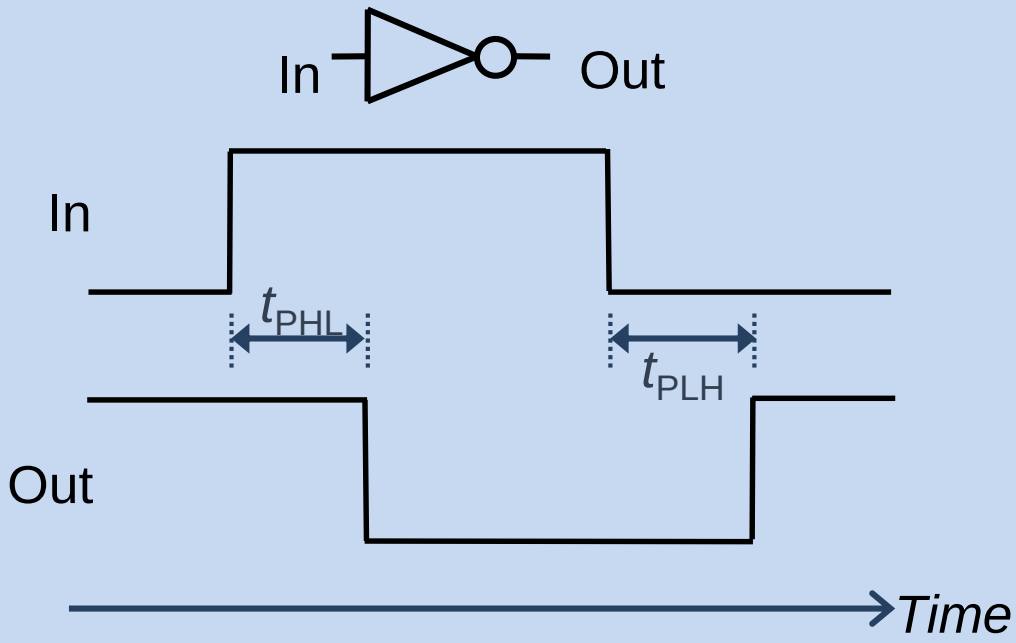
57218 & 57092

Digital Electronics

Dr Ian M. Bell

Logic in the Real World - Speed

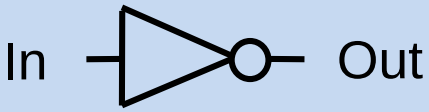
- Logic gates take time to react to changes on their inputs
- Time from input changing to output reacting is the **propagation delay t_P**
- Propagation delays may differ depending direction of change of the output
  - ❑ t_{PHL} **Propagation delay high-to-low** (output change 1 to 0)
  - ❑ t_{PLH} **Propagation delay low-to-high** (output change 0 to 1)



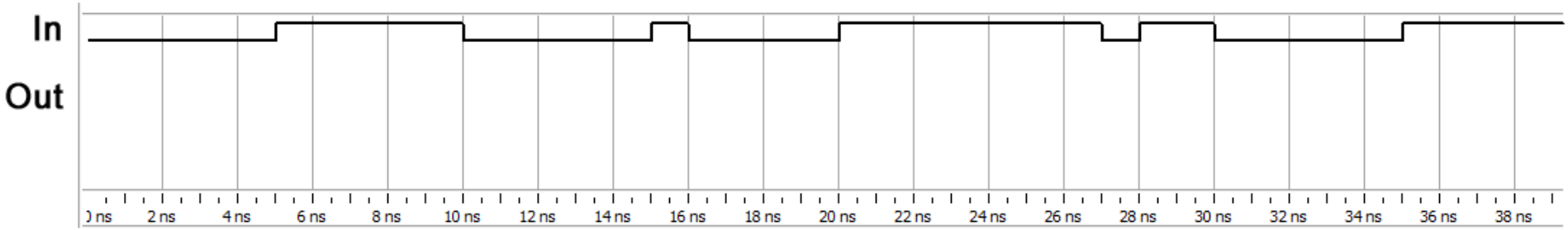
Timing diagrams are used to depict the timing of digital circuits

Logic in the Real World - Speed

Draw the output waveform

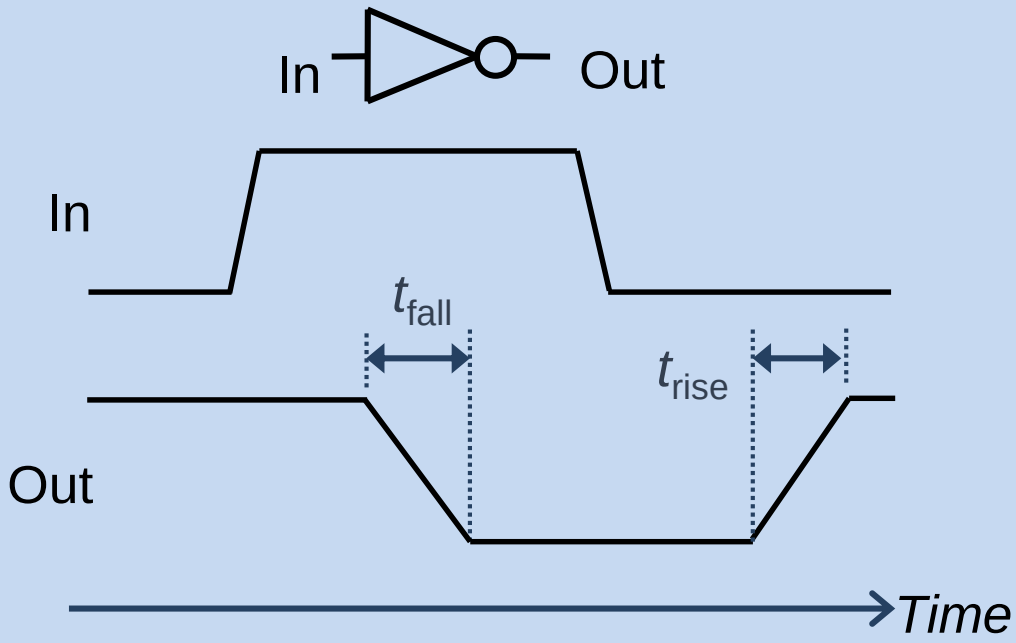


Propagation delay 2 ns



Logic in the Real World - Speed

- Logic voltages on gate outputs do not change instantaneously when the logic level change
- Time for output to change from one state to another is the **transition time t_T**
- Transition times may differ depending direction of change of the output
  - ❑ t_{fall} **Fall time** (output change 1 to 0) also called **transition time high to low t_{THL}**
  - ❑ t_{rise} **Rise time** (output change 0 to 1) also called **transition time low to high t_{TLH}**



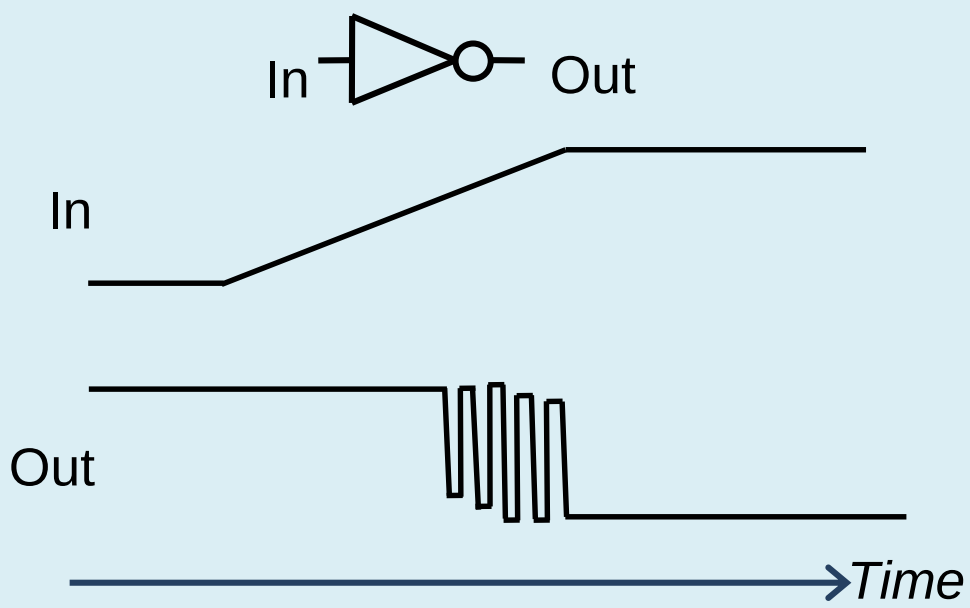
Inputs have transition times too, but we are interested in the output, which characterises the gate

For simplicity accurate transition times are often not shown on timing diagrams

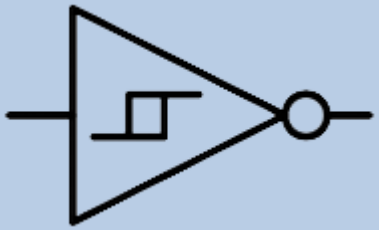
Problems with slow transitions

- Slow edges on logic gate inputs may cause problems
  - For example erratic multiple switching of outputs
- What constitutes “slow” depends on the logic family (also supply voltage etc.)
- Problems can occur when attempting to drive the input of “fast” logic family from one with a relatively slow output.

Multiple output transitions due to slow input transition



In cases where slow inputs cannot be avoided **Schmitt trigger** gates, specially designed to cope with slow edges, can be used. They use positive feedback to ensure more definite switching



Schmitt trigger NOT Gate symbol

Summary of Timing Parameters

Edge Timing

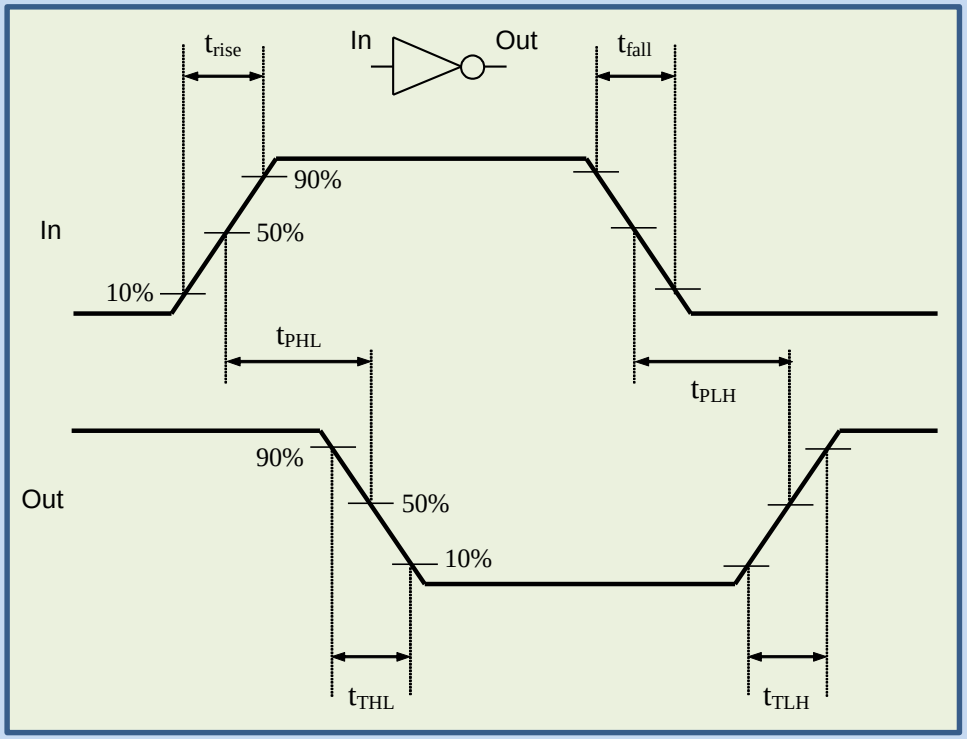
t_r Rise Time

t_f Fall Time

t_{TLH} Transition time low-to-high

t_{THL} Transition time high-to-low

Edge times typically measured from 10% to 90% points of transition



Input-to-Output Timing

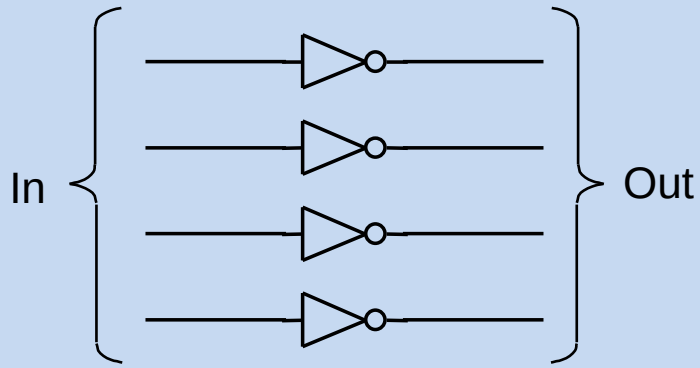
t_{PLH} Propagation delay low-to-high

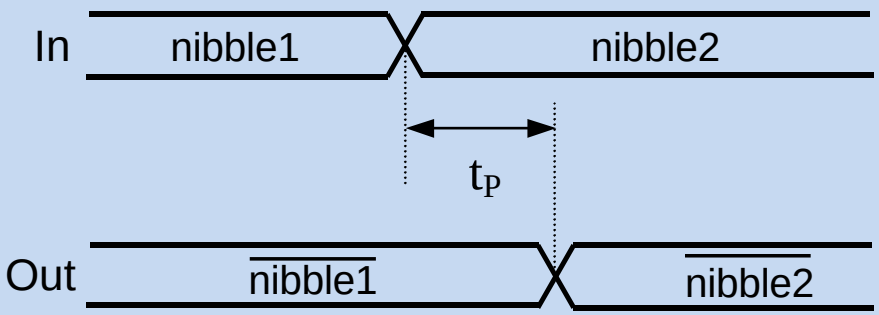
t_{PHL} Propagation delay high-to-low

t_P Propagation delay (average of t_{PLH} and t_{PHL})

Propagation delays typically measured from 50% points of transition, or a defined logic threshold voltage

Timing Diagrams for Multi-bit Signals

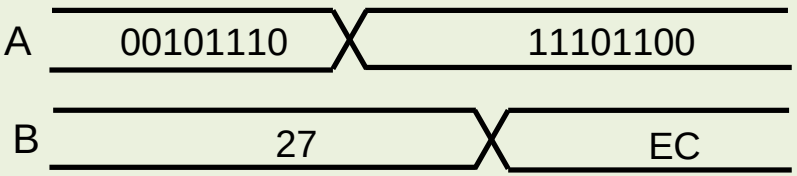




Names for collections of bits

Bit	Binary Digit 0 or 1
Byte	8 bits
Nibble	4 bits
Word	Specified number of bits

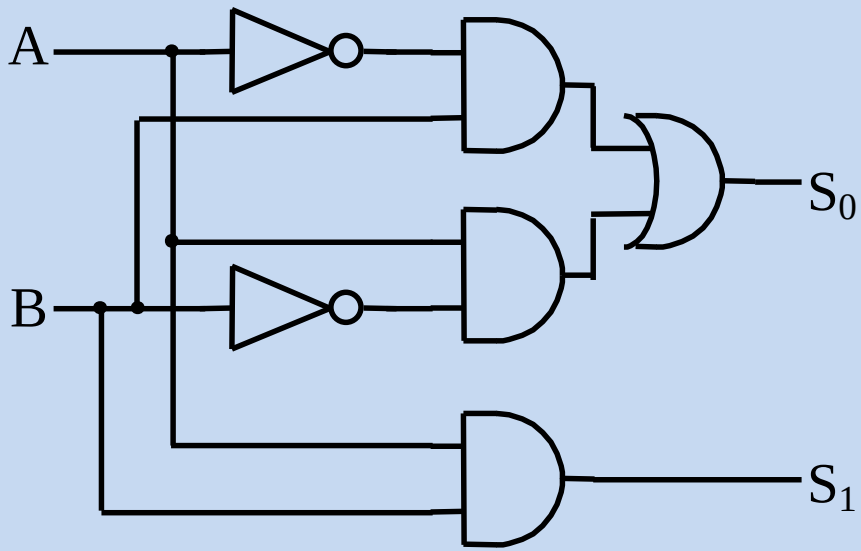
- **Signal values may be shown in binary, decimal, hexadecimal etc**
- **Crossovers do not usually represent actual rise and fall times**



Timing in Multiple-Output Circuits

If A stays at 1 and B changes from 0 to 1, both outputs change

Which output changes first? (all gates have the same propagation delay)



A_0	B_0	S_0
0	0	0
0	1	1
1	0	1
1	1	0

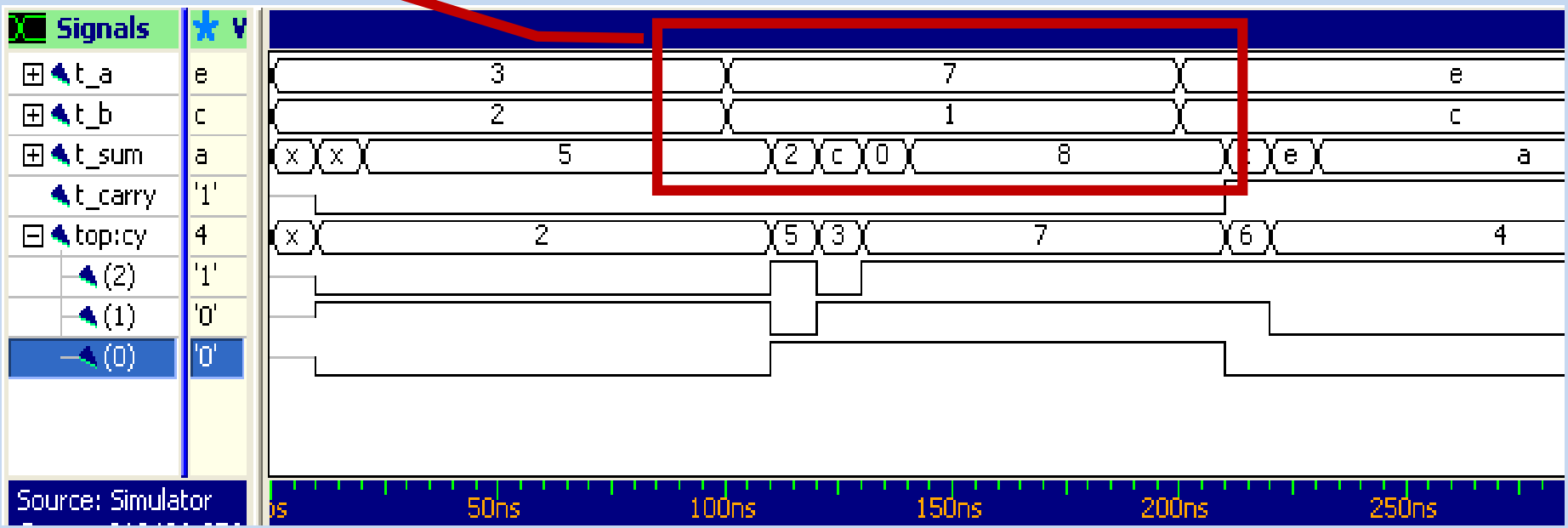
A_0	B_0	S_1
0	0	0
0	1	0
1	0	0
1	1	1

Again We have to be careful that intermediate states which occur as circuits switch do not cause incorrect behaviour in other parts of the circuit

Simulation Example Showing Circuit Settling to Correct Value

Adder circuit adding two 4-bit binary numbers t_a and t_b to give t_sum

Example: adding 1+7 produces 2, C and 0 before the adder settles to the correct value of 8



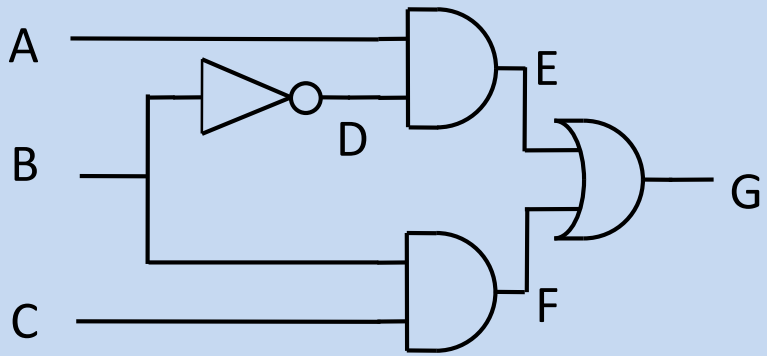
Intermediate values taken as a circuit responds are usually shown by simulators, sometimes confusing new users who expect to see "clean" changes.

As a digital designer you need to be able to interpret timing diagrams (waveforms) obtained by circuit simulation.

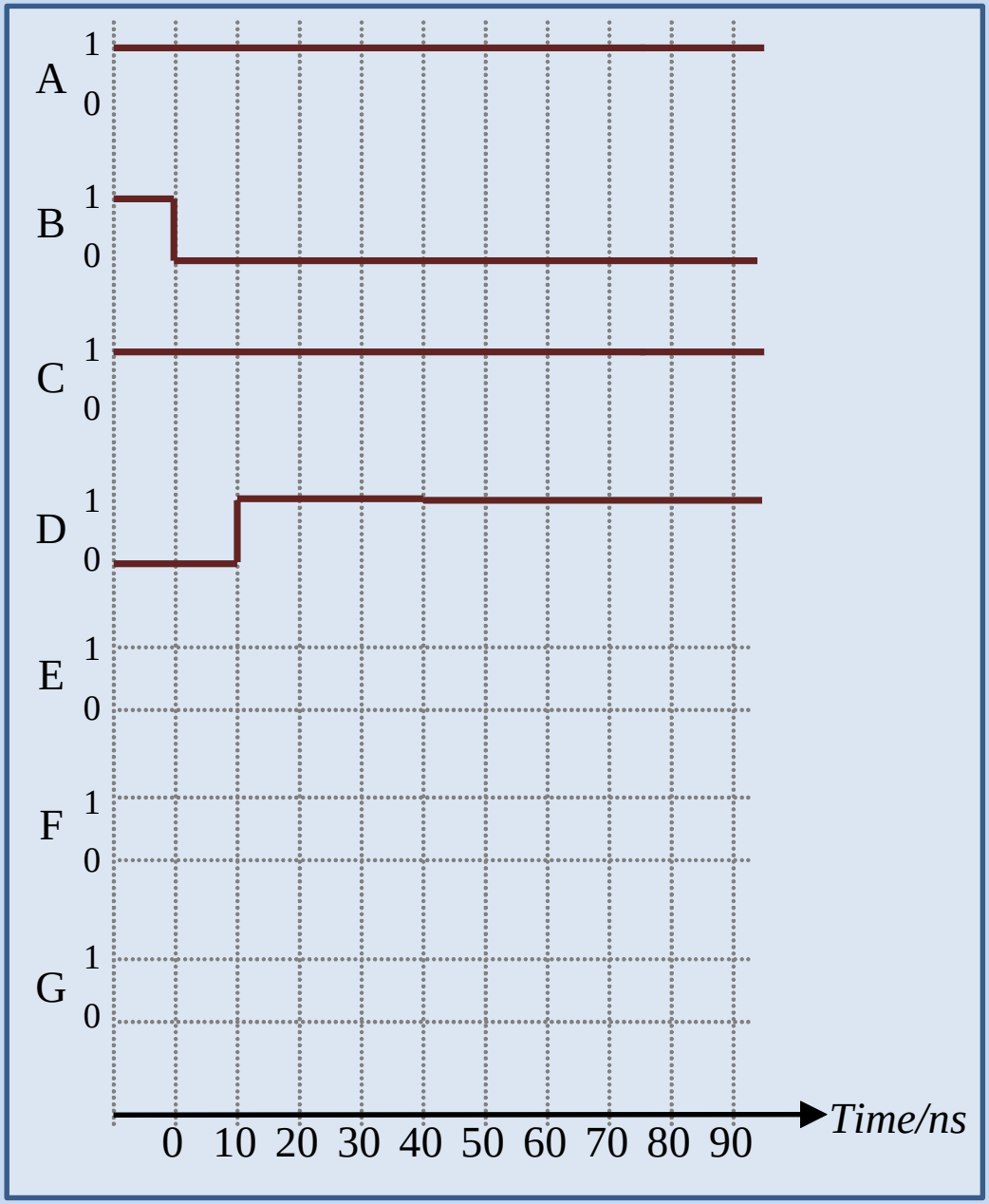
Delays in a Circuit - Example

What happens if the input changes from ABC=111 to ABC=101 after being at ABC=111 for a long time?

Delay = 10ns for all gates



The waveform for D is already shown. In a similar way draw the waveforms for E, F and G



Glitches and Hazards

Unwanted switching activity at circuit outputs, which occurs when inputs change

- **Glitch** – unwanted pulse on a logic output
- **Static Hazard** – when output should stay at the same value
- **Dynamic Hazard** – when output should change 0 to 1 or 1 to 0

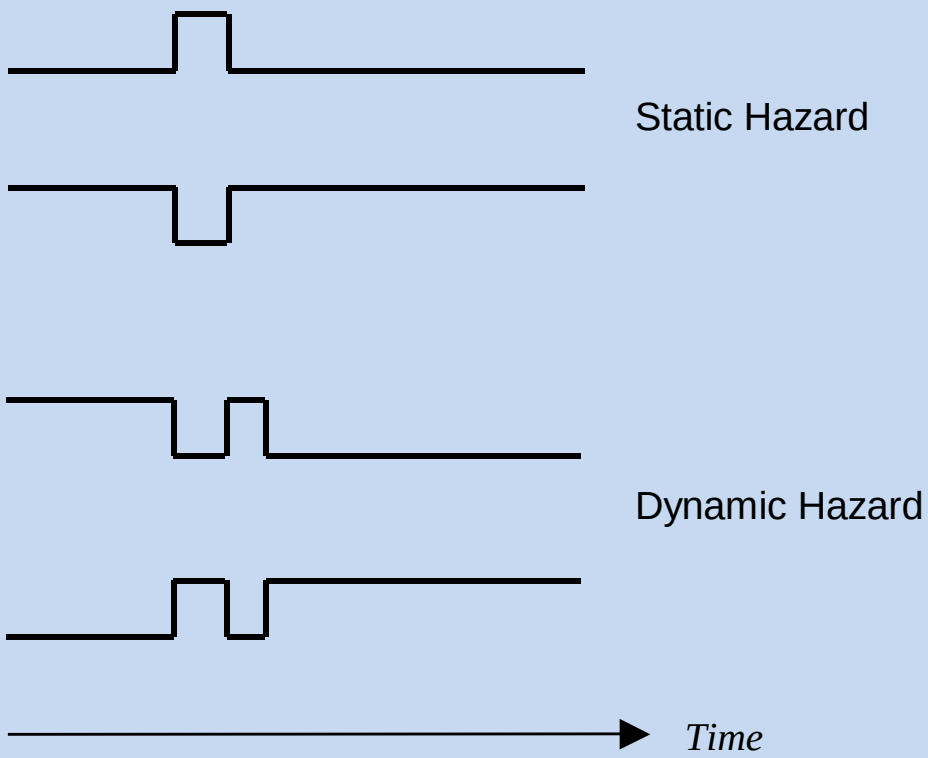
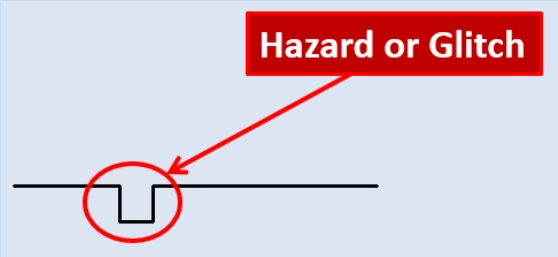
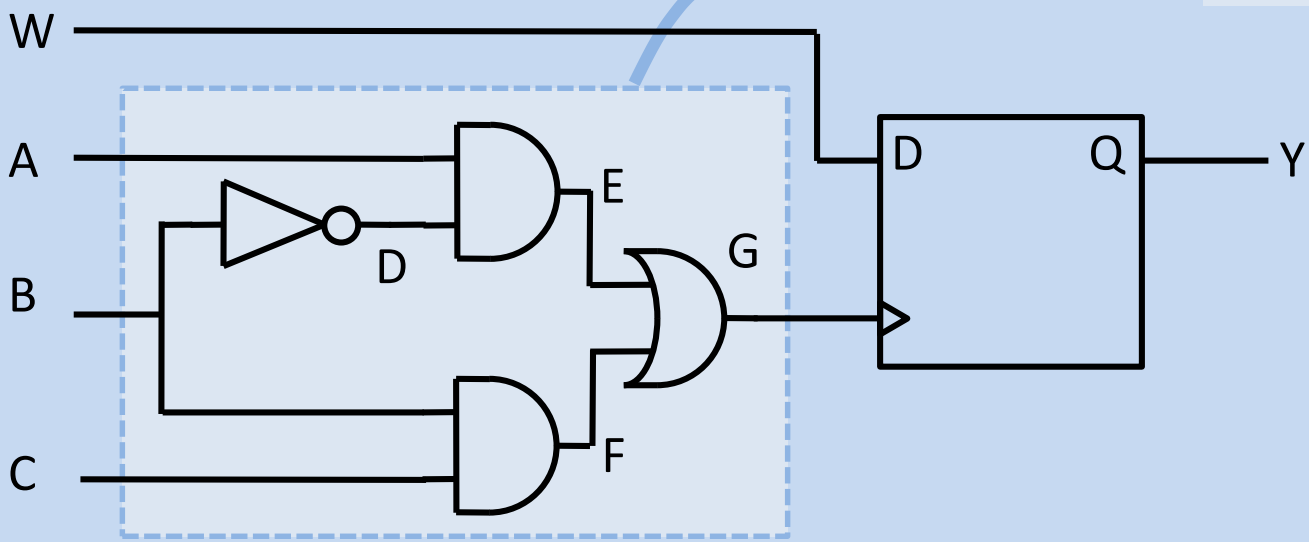


Diagram shows logic outputs for example static and dynamic hazard situations

Glitches and Hazards – Avoiding Problems

What might go wrong in this circuit?



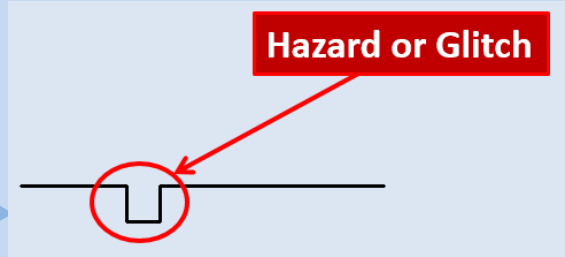


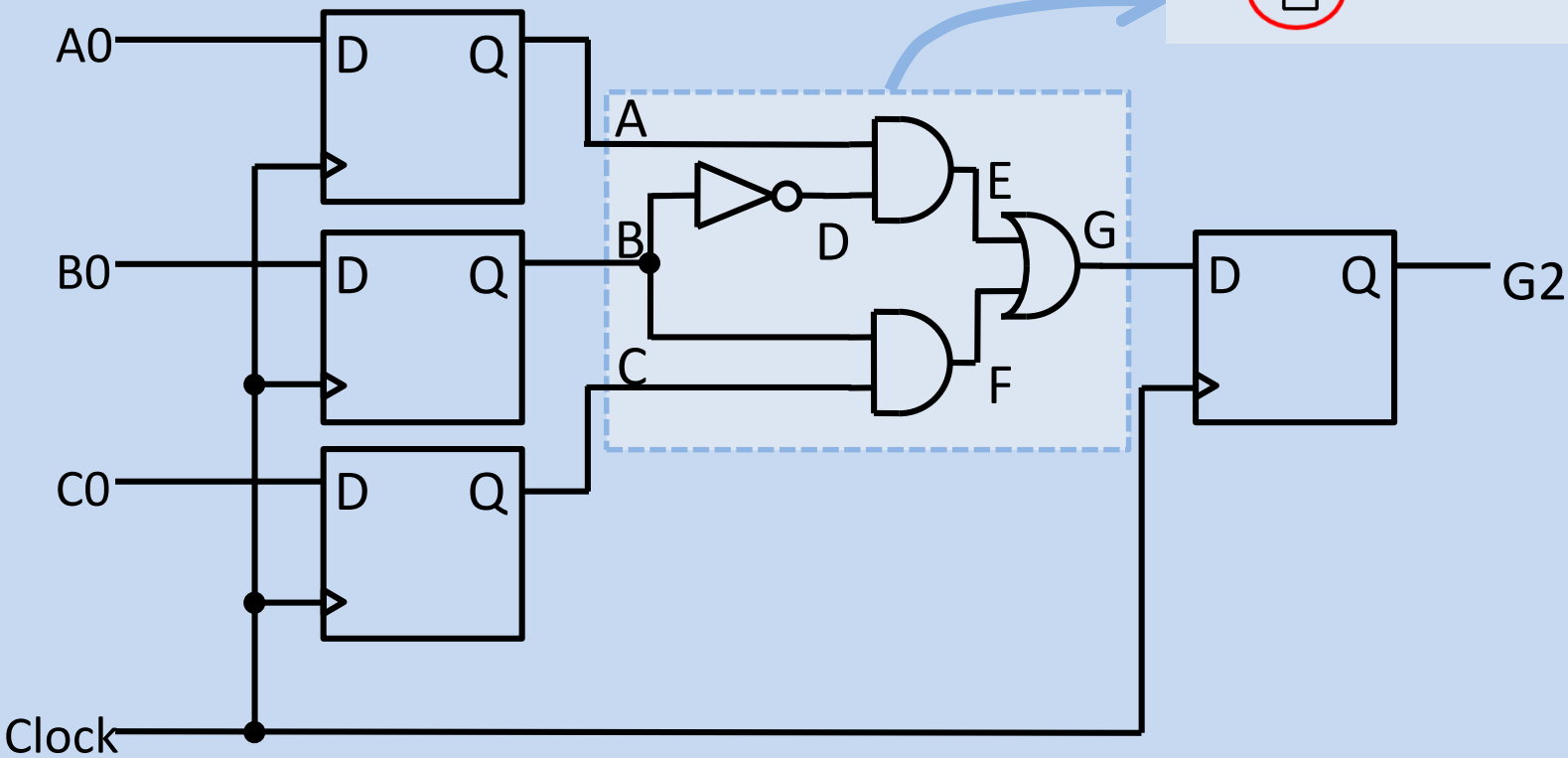
If a circuit which may produce a glitch is connected to the clock of a flip flop, the flip flop may get clocked by the glitch, causing it to store a wrong value

To avoid problems this must not be done!

Delay, Glitches and Hazards – Avoiding Problems

How do we prevent glitches, or settling time of the combination logic in general, from causing problems in this circuit?





If the rate at which the flipflops are clocked is slower than the time taken for the combinational logic to settle the output flopflops will always load the correct value

Digital Circuits – Memory and Combinational Logic

- Large digital circuits typically comprise sets of registers (R), built from flipflops, interconnected via combinational logic (CL)
- The values stored in the registers are updated under control of a **clock** signal sent to each memory
- The clock is typically a square wave

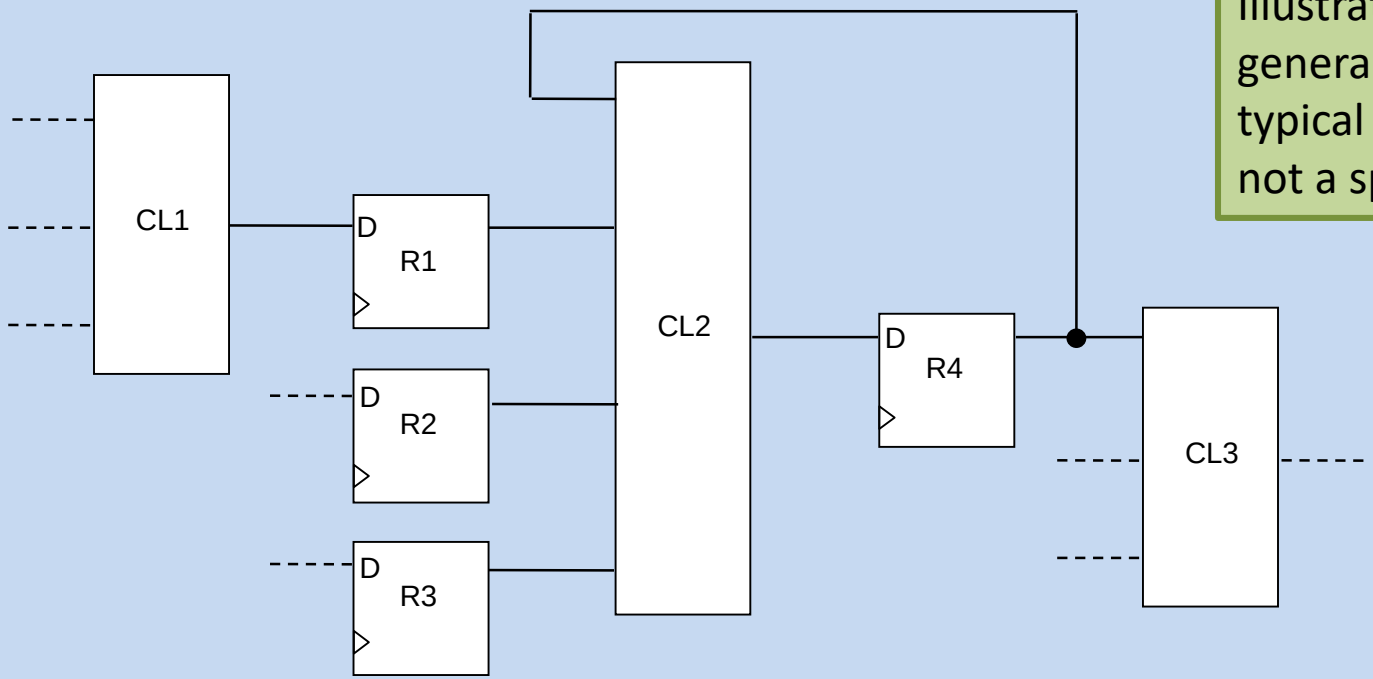
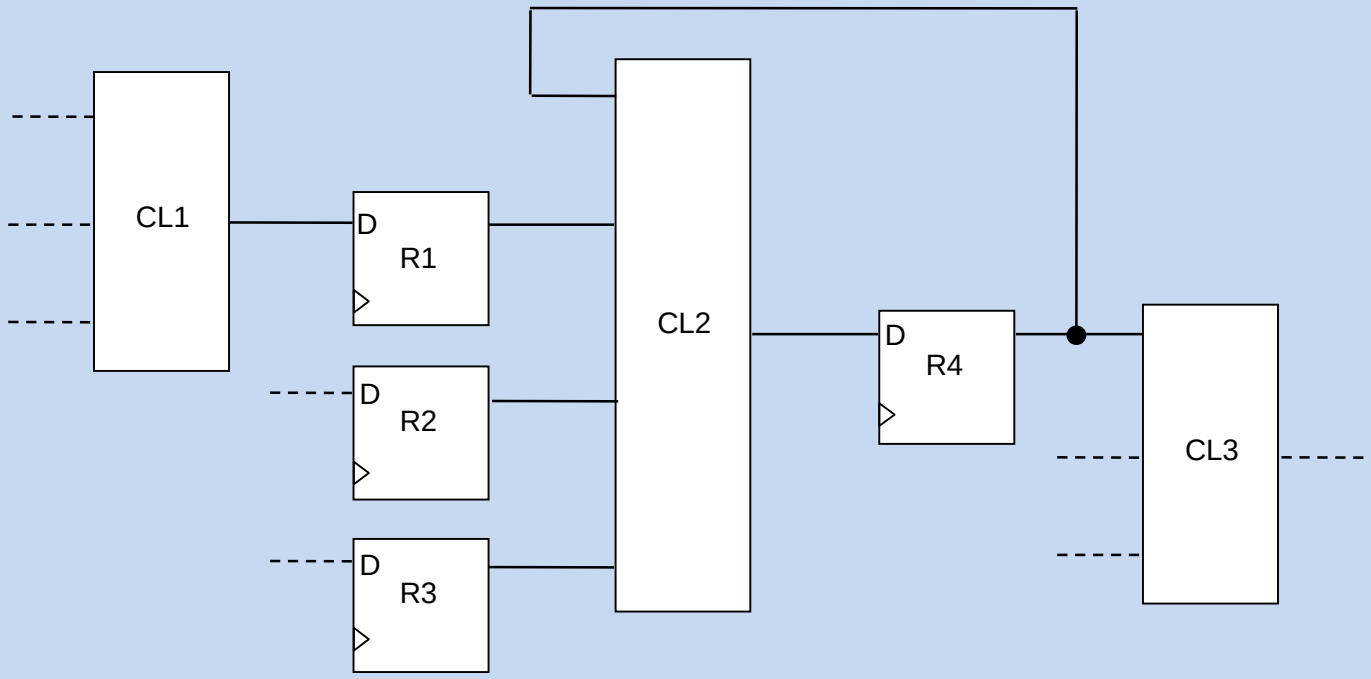


Illustration of the general structure of a typical circuit – this is not a specific function

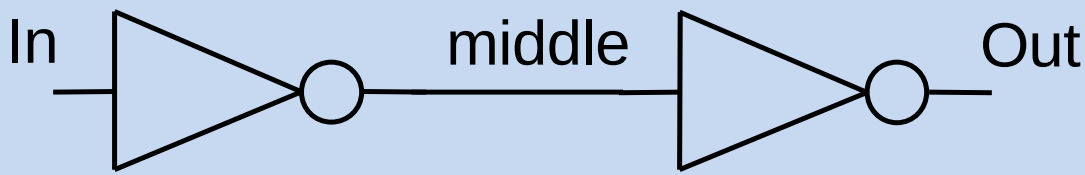
Important timing requirements for Digital Circuits

- If the time between updates of the memory elements (flip flops) is greater than the time taken for the combinational logic to settle down we do not have to worry about glitches and hazards
- Logic which can produce glitches must not be connected to clock inputs as it may cause unwanted extra clocks



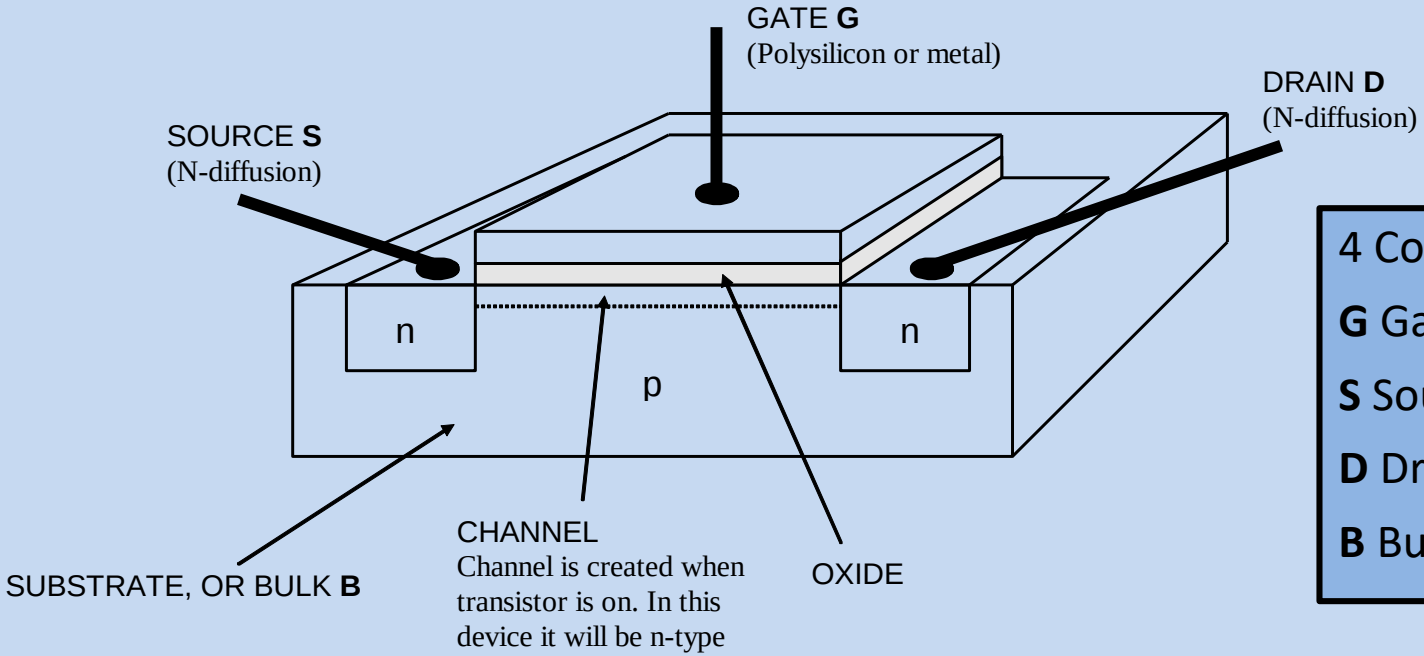
CMOS Inverter Delay

- By studying the internal circuitry of the inverter (NOT gate) we gain understanding of where delays come from
- *Two* inverters in series are useful for studying delay
- The second inverter acts as a load for the second. This loading has an important influence on delay



- Before performing an analysis of the delay we will look at the MOSFET again
- We will also need to look at some basic circuit theory for resistors and capacitors

Simplified Structure of an N-Channel MOSFET Transistor



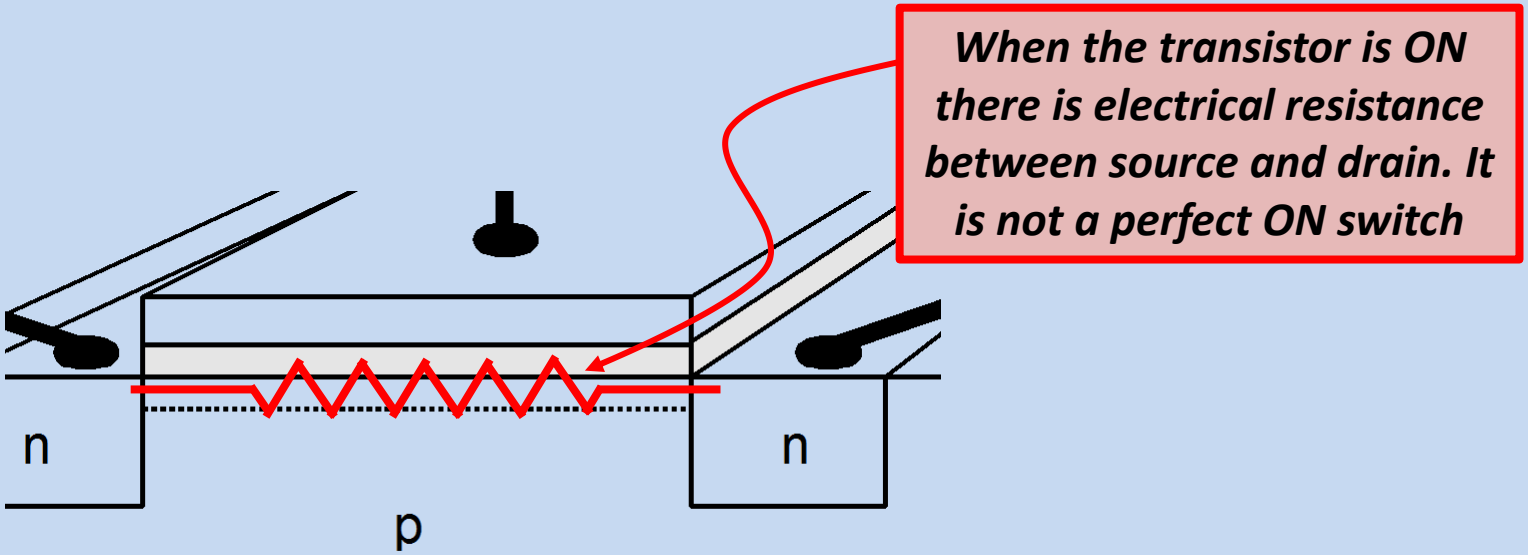
4 Connections:

G Gate

S Source

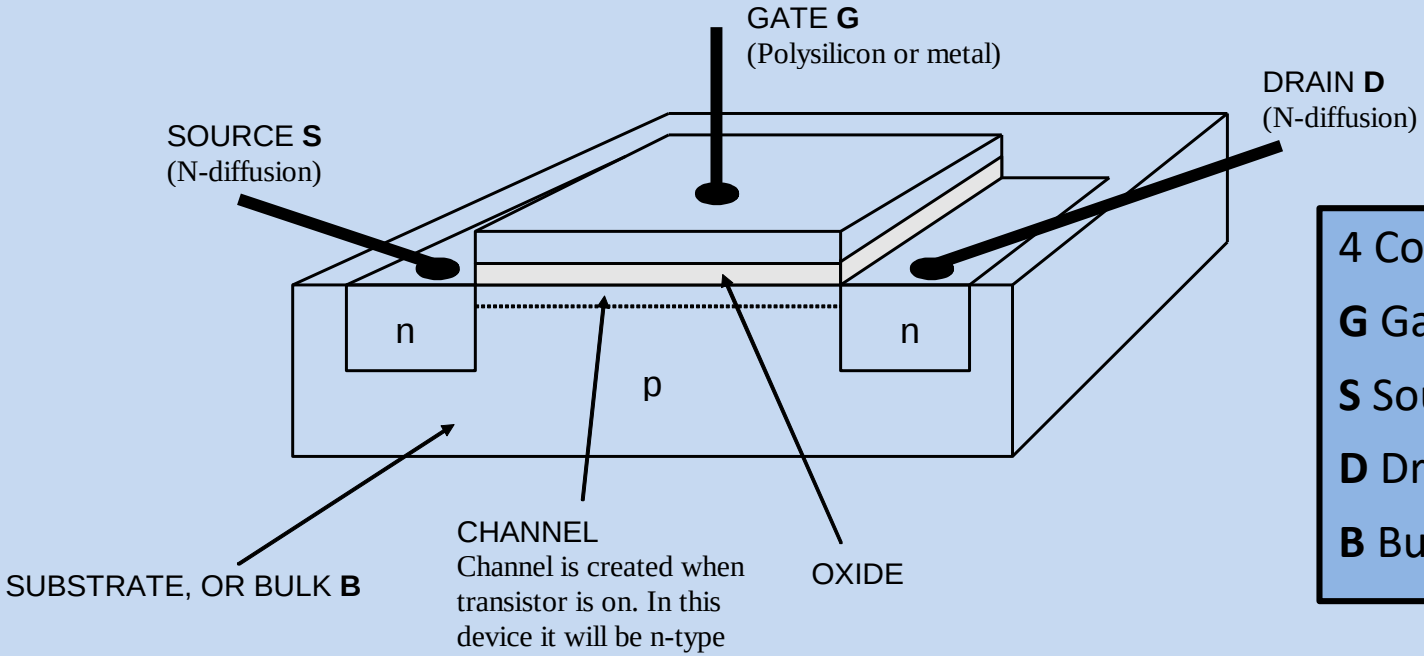
D Drain

B Bulk or Substrate



When the transistor is ON there is electrical resistance between source and drain. It is not a perfect ON switch

Simplified Structure of an N-Channel MOSFET Transistor



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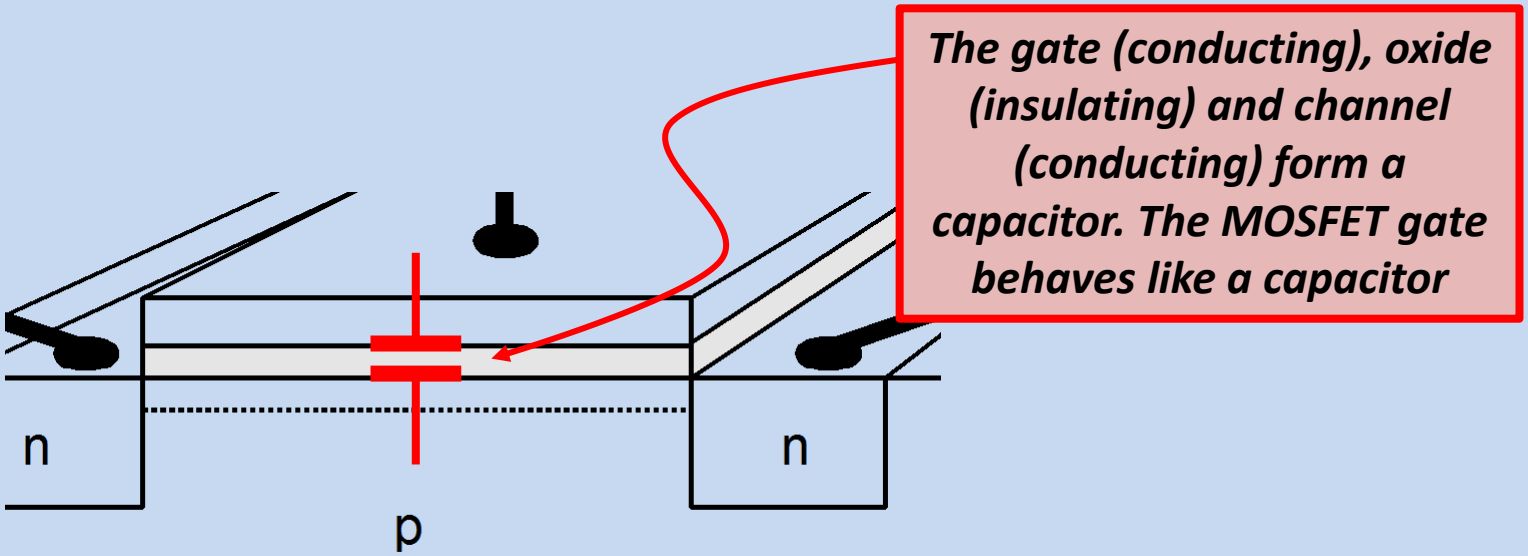
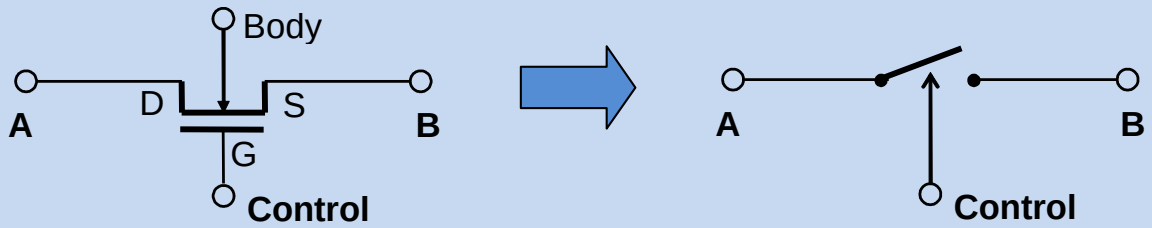


The gate (conducting), oxide (insulating) and channel (conducting) form a capacitor. The MOSFET gate behaves like a capacitor

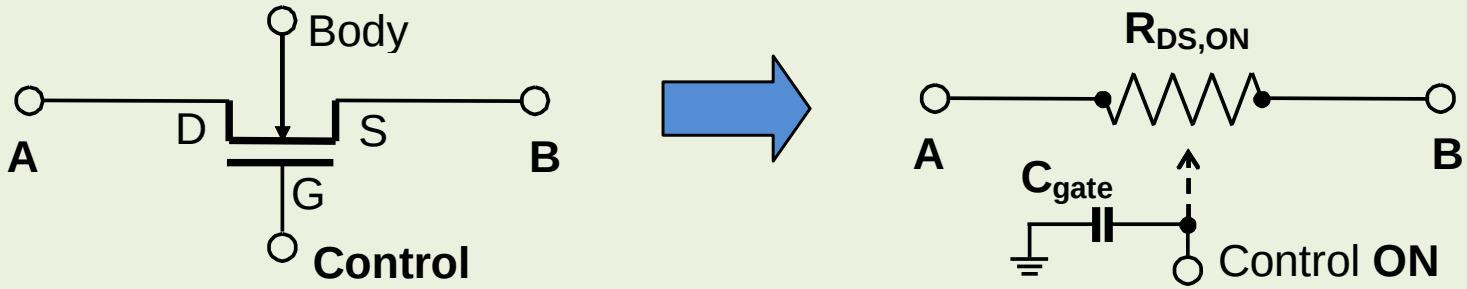
Building Logic Gates - The transistor as a switch

Transistor circuit *Ideal equivalent circuit*

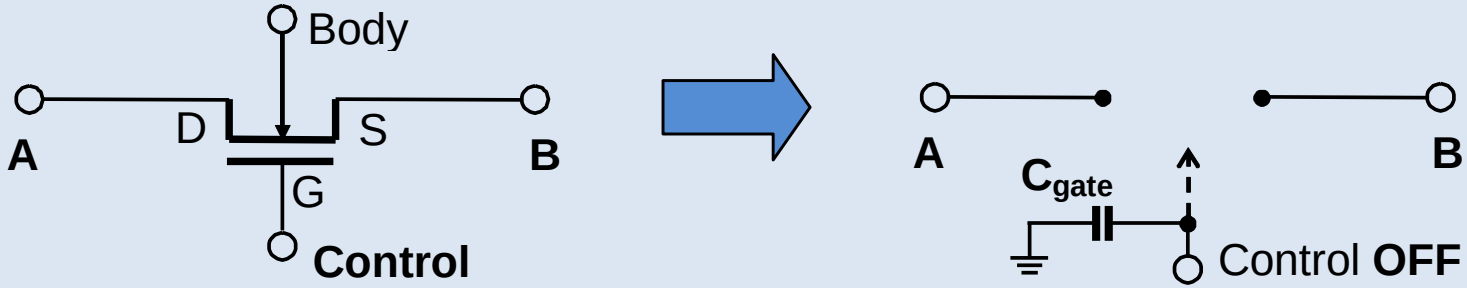


- **The switch is not perfect - we need a more accurate equivalent circuit**
  - when it is on it has non-zero resistance (drain to source), unlike a real switch
  - The control input (gate) has capacitance

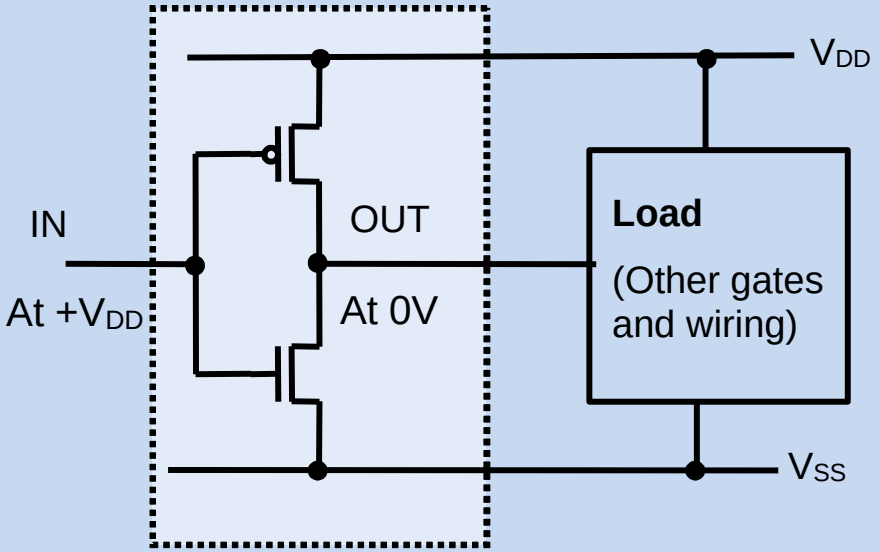
ON



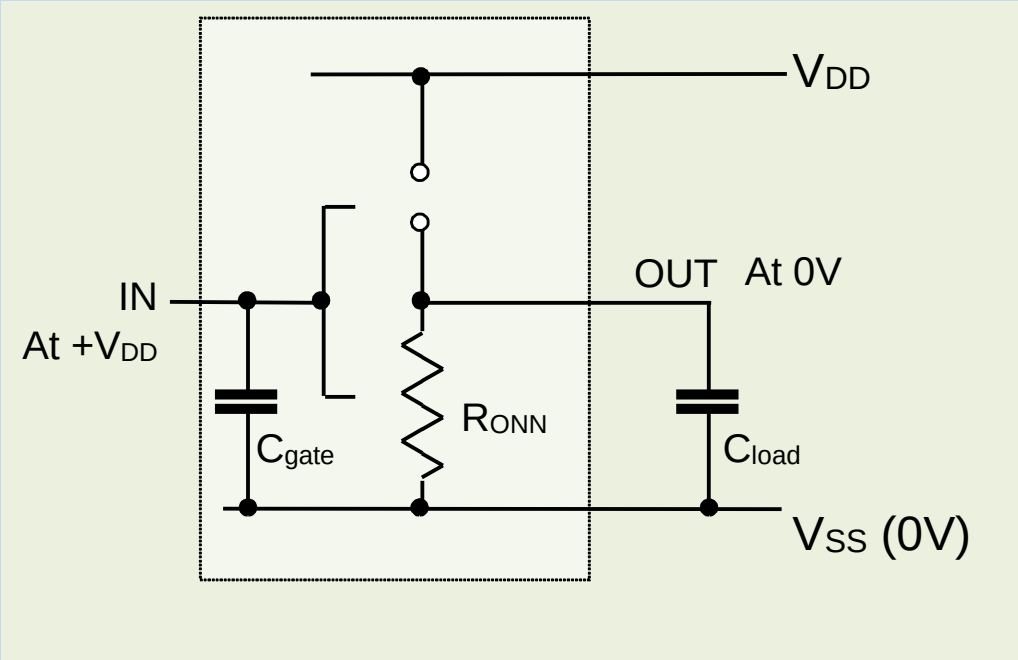
OFF



Equivalent circuit of inverter (with 1 on input 0 on output)

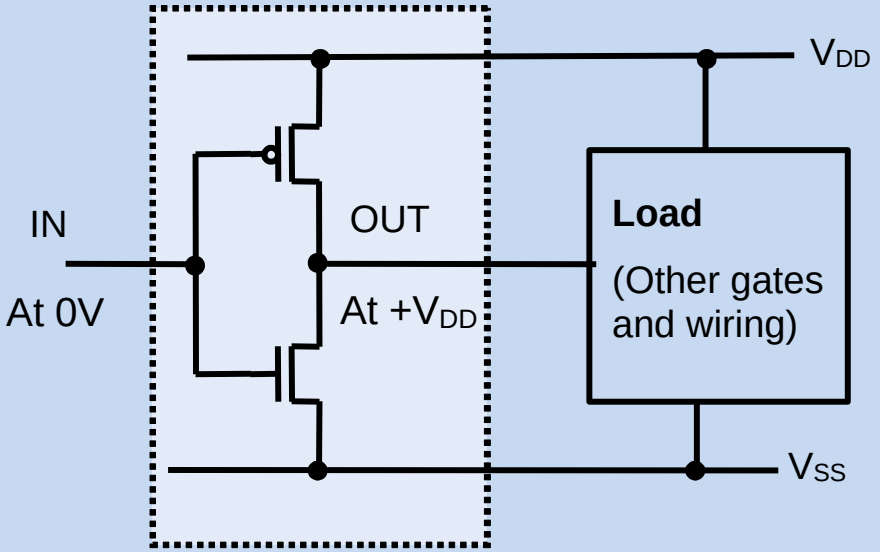


- **Inverter input** equivalent to a capacitor
- **Inverter output** equivalent to a resistor at the position of transistor which in on
- **Load** equivalent to a capacitor (other gate inputs and wiring)



- Assume circuit has been like this for a long time
- IN currently at $+V_{DD}$
- OUT is at 0V
- C_{load} has fully discharged through R_{ONN}

Equivalent circuit of inverter (with 0 on input 1 on output)



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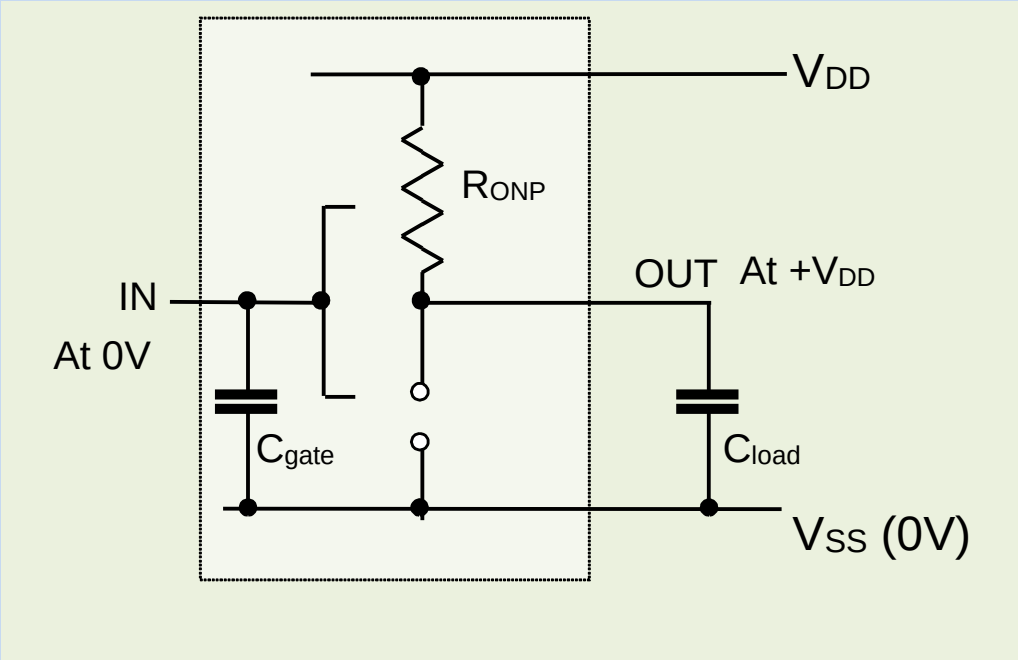


- Assume circuit has been like this for a long time
- IN currently at 0V
- OUT is at $+V_{DD}$
- C_{load} has fully charged through R_{ONP}

A note on V_{DD} and V_{SS}

V_X is the voltage on the wire labelled ***X*** measured with respect to ground

V_Y is the voltage on the wire labelled ***Y*** measured with respect to ground

V_{XY} = V_X - V_Y is the voltage measured between wires ***X*** and ***Y*** with Y as the reference point

V_{XX} is a power supply voltage. Note the interpretation $V_{XX} = V_X - V_X = 0$ is not needed so we are free to assign another meaning to V_{XX}

Supply voltages in FET circuits are often written as

V_{DD} positive supply (drain supply, NMOS)

V_{SS} negative supply or ground (source supply, NMOS)

- Double subscript naming convention for supplies originates from 1963 IEEE standard 255-1963 "Letter Symbols for Semiconductor Devices“.

Capacitor Charging through a Resistor

We have seen that when CMOS gate switches the load capacitance is charged or discharged via the gate's output transistor(s)

To analyse the timing in more depth we need to know about the timing of capacitors charging and discharging via resistors

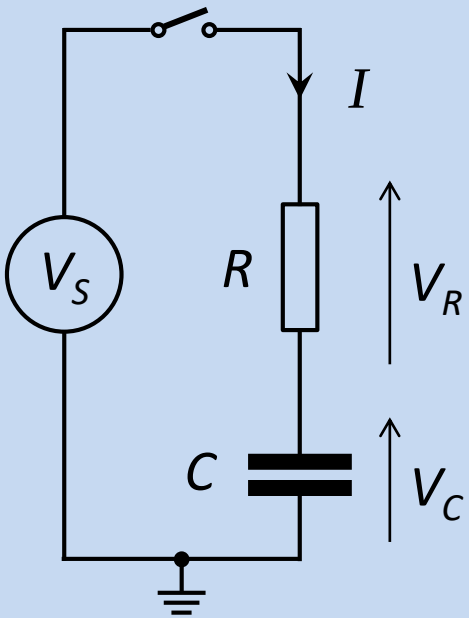
A simplified approach will be used here

- Intuitive description
- Equations presented without formal derivation

The topic will be covered in more depth in 57217 / 57022

- Transient processes/analysis in RC and RL circuits

Capacitor Charging through a Resistor



$$I = V_R / R$$

$$I = (V_S - V_C) / R$$

Assume C starts with no charge ($\boldsymbol{Q_C = 0}$, $\boldsymbol{V_C = 0}$)

When switch closes current flows, adding charge to the capacitor

At the instant the switch closes $\boldsymbol{V_C = 0}$ so $\boldsymbol{I = V_S / R}$

As charge accumulates on the capacitor the voltage across it will increase $\boldsymbol{V_C = Q_C / C}$

As $\boldsymbol{V_C}$ increases $\boldsymbol{V_R}$ must decrease ($\boldsymbol{V_R = V_S - V_C}$)

As $\boldsymbol{V_R}$ decreases $\boldsymbol{I}$ must also decrease ($\boldsymbol{I = V_R / R}$)

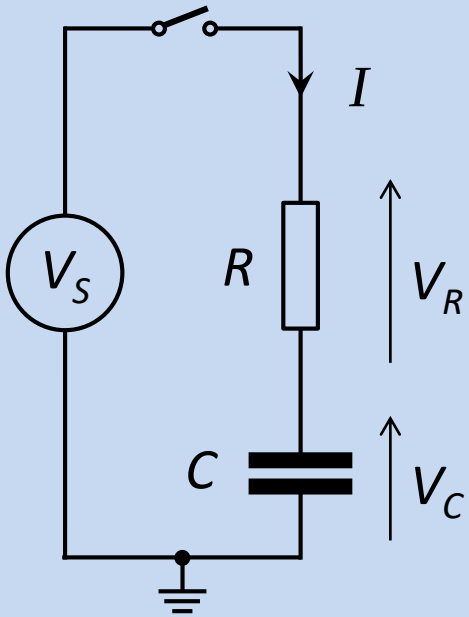
As the capacitor charges the current decreases (i.e. as time moves on the current decreases)

Current defined by $\boldsymbol{I = \Delta Q / \Delta t}$ so as the current decreases the rate at which charge is added to the capacitor decreases

As $\boldsymbol{V_C = Q_C / C}$ we can write $\boldsymbol{\Delta V_C = \Delta Q_C / C}$, so the **rate of increase in voltage** across the capacitor **decreases** as time moves on

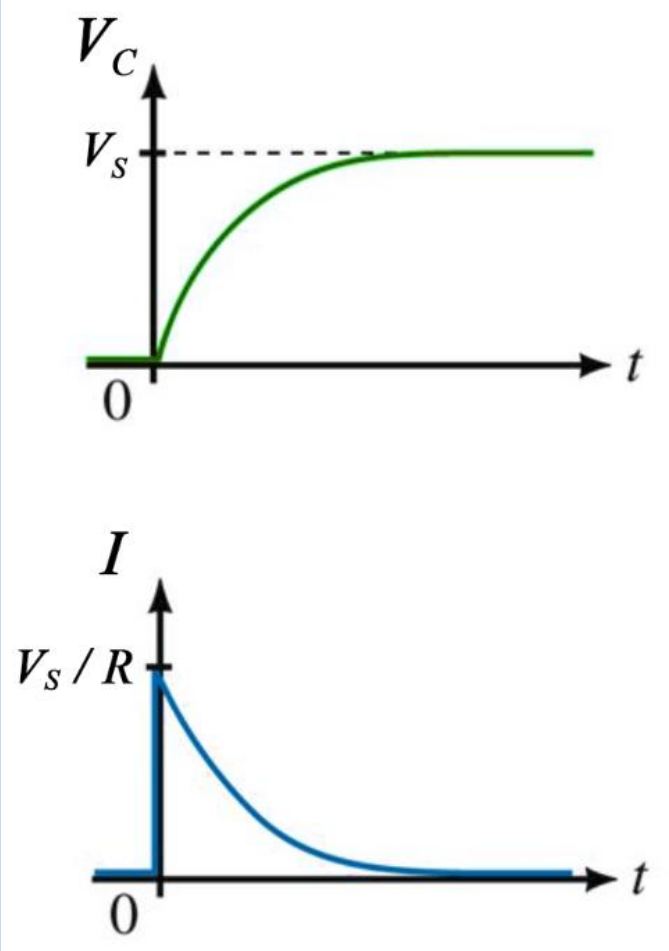
Maximum $\boldsymbol{V_C}$ is $\boldsymbol{V_S}$ (capacitor fully charged, $\boldsymbol{I = 0}$)

Capacitor Charging through a Resistor



Voltage and current waveforms

Switch is closed at time t=0

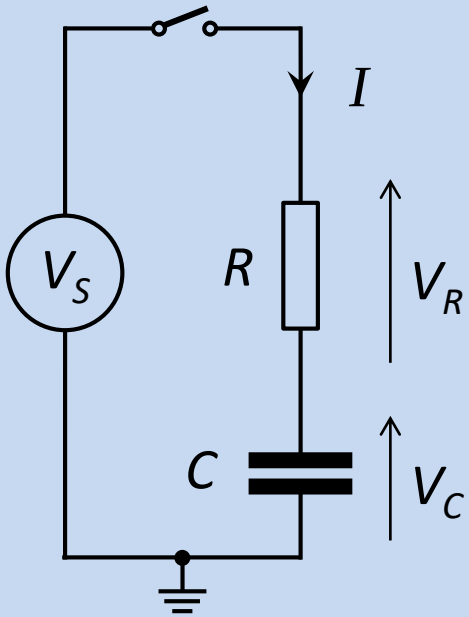


After switch is closed

$\boldsymbol{V_C}$ increases as capacitor charges. Rate of change decreases with time. Final voltage is asymptotic to $\boldsymbol{V_S}$

$\boldsymbol{I}$ decreases as capacitor charges. Rate of change decreases with time. Final current is asymptotic to zero

Capacitor Charging through a Resistor



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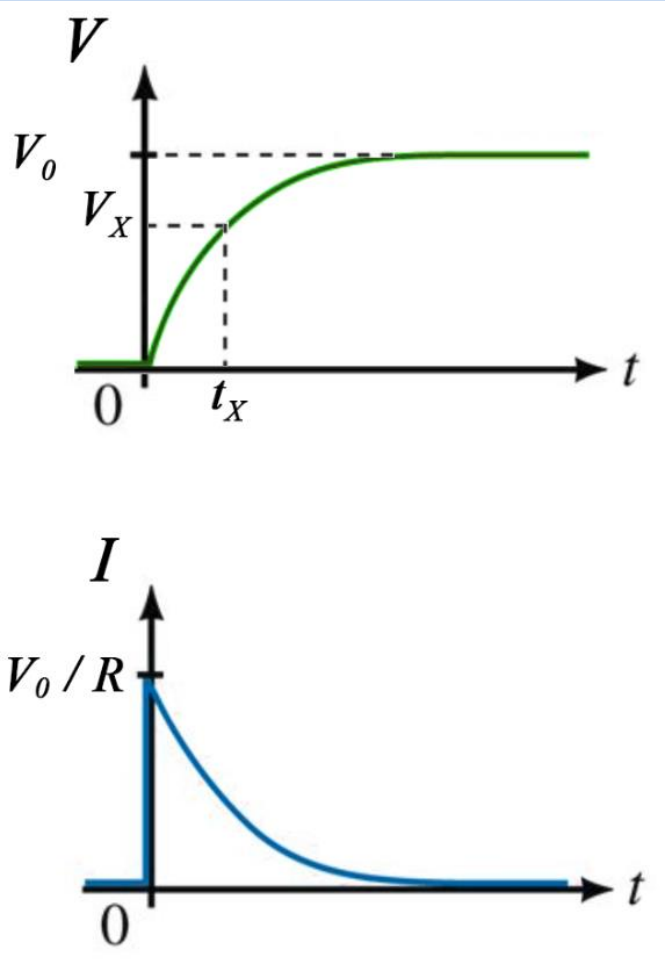
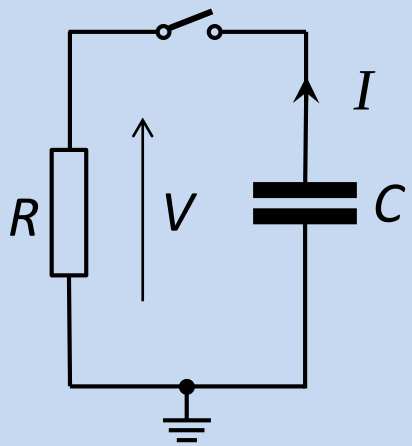


Time $\boldsymbol{t_X}$ taken to reach voltage $\boldsymbol{V_X}$

Capacitor starts at 0V

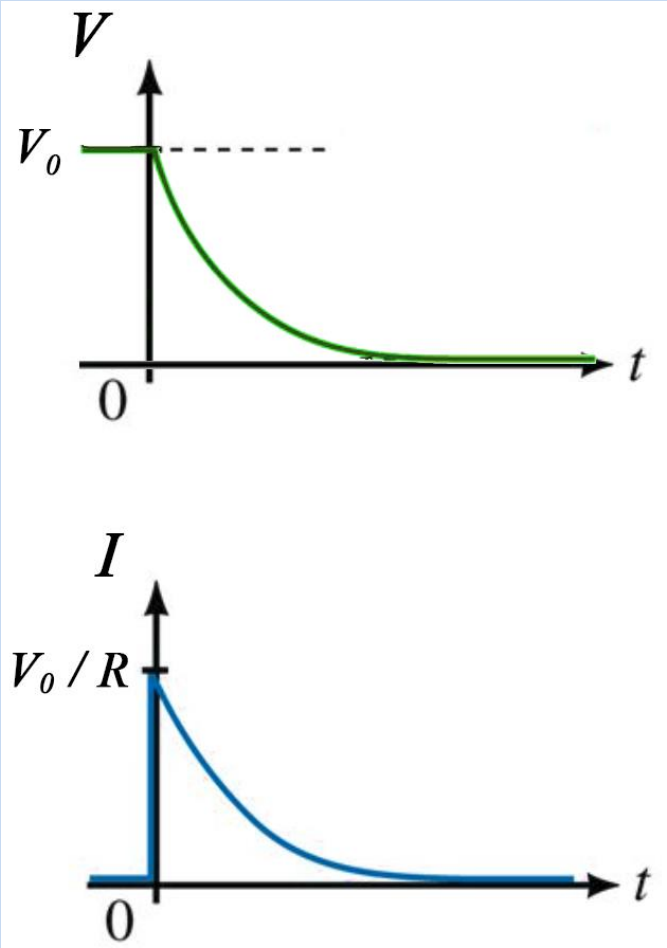
$$t_X = -RC\ln\left(1-\frac{V_X}{V_S}\right)$$

Capacitor Discharging through a Resistor



Voltage and current waveforms

Switch is closed at time t=0



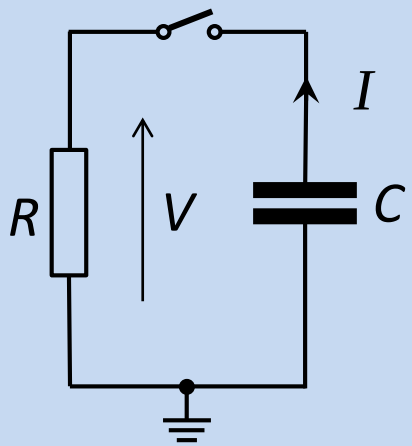
Before switch is closes capacitor is charged to voltage V_0

After switch is closed

V decreases as capacitor discharges. Rate of change decreases with time. Final voltage is asymptotic to zero

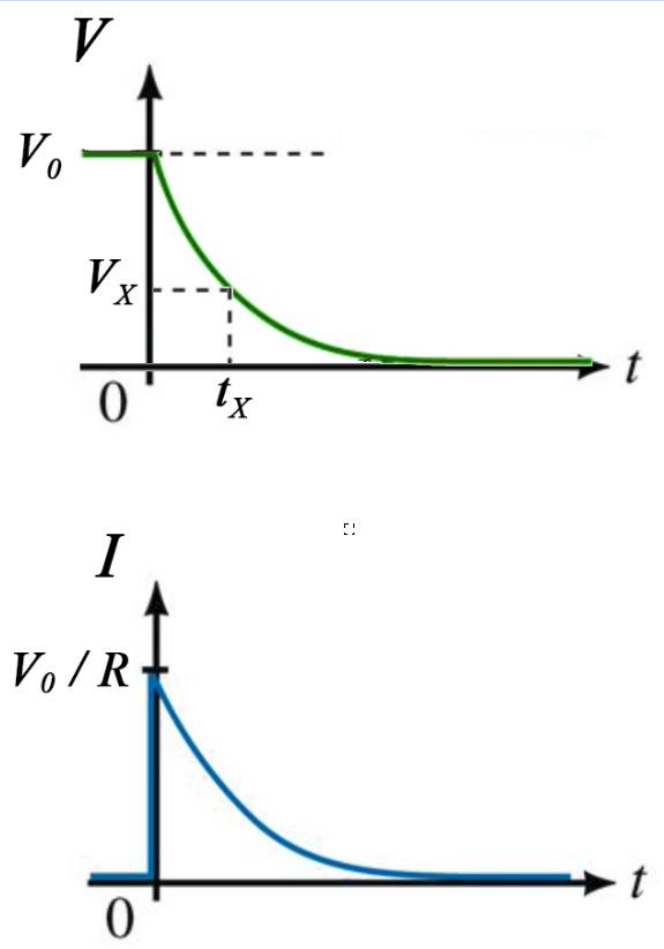
I decreases as capacitor discharges. Rate of change decreases with time. Final current is asymptotic to zero

Capacitor Discharging through a Resistor



Voltage and current waveforms

Switch is closed at time t=0



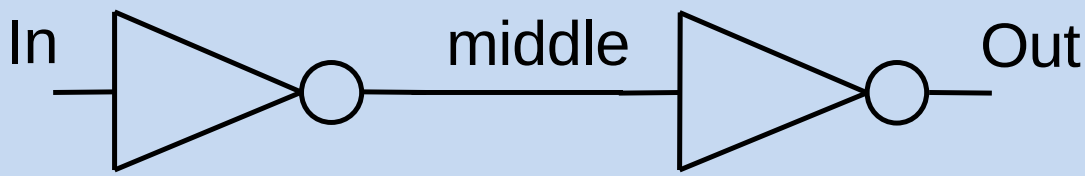
Time t_X taken to reach voltage V_X

Capacitor starts at V_0

$$t_X = -RC \ln\left(\frac{V_X}{V_0}\right)$$

CMOS Inverter Delay

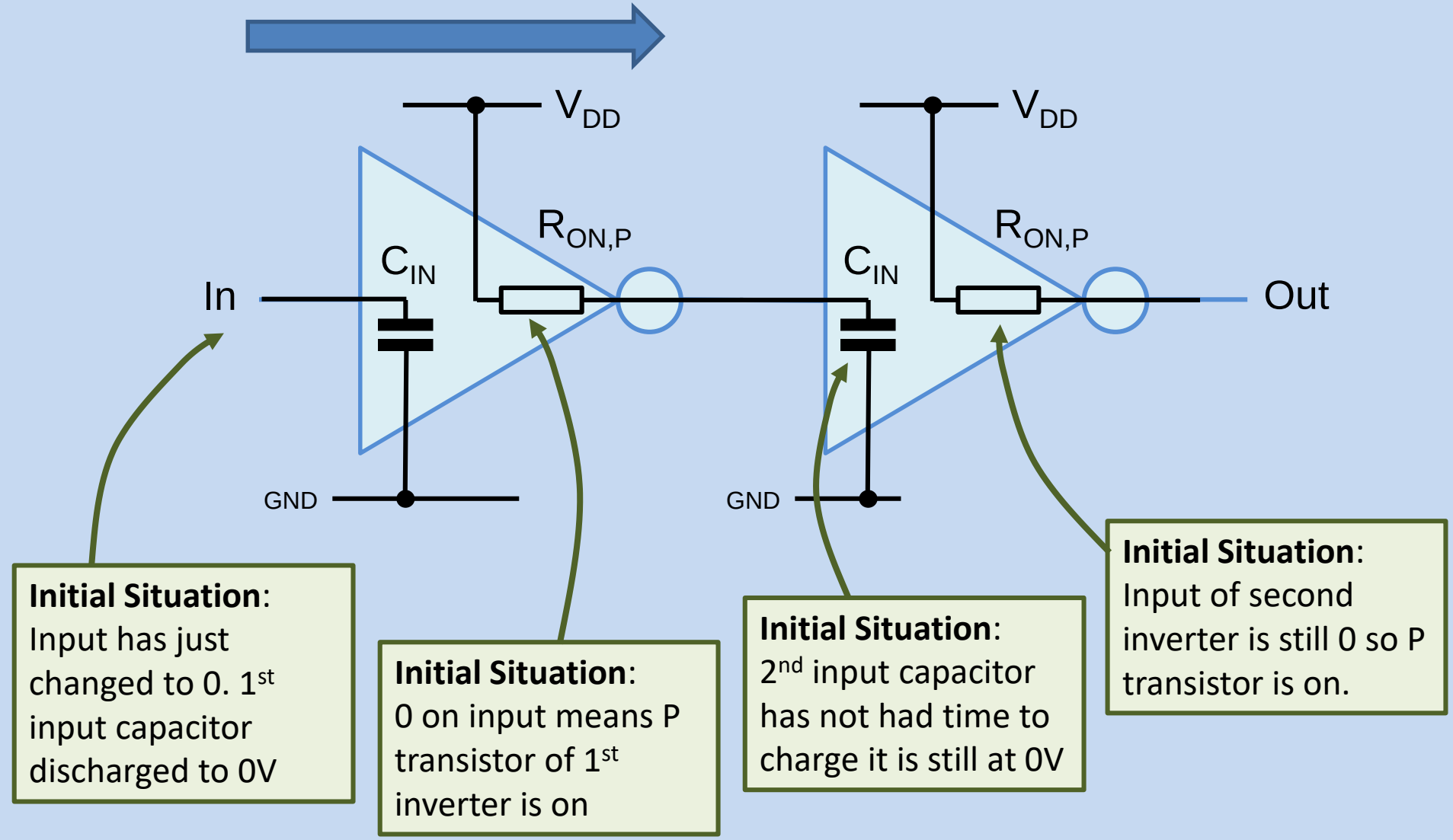
- By studying the inverter we gain understanding of where delays come from
- *Two* inverters in series are useful for studying delay
- The second inverter acts as a **load** for the second. This loading has an important influence on delay



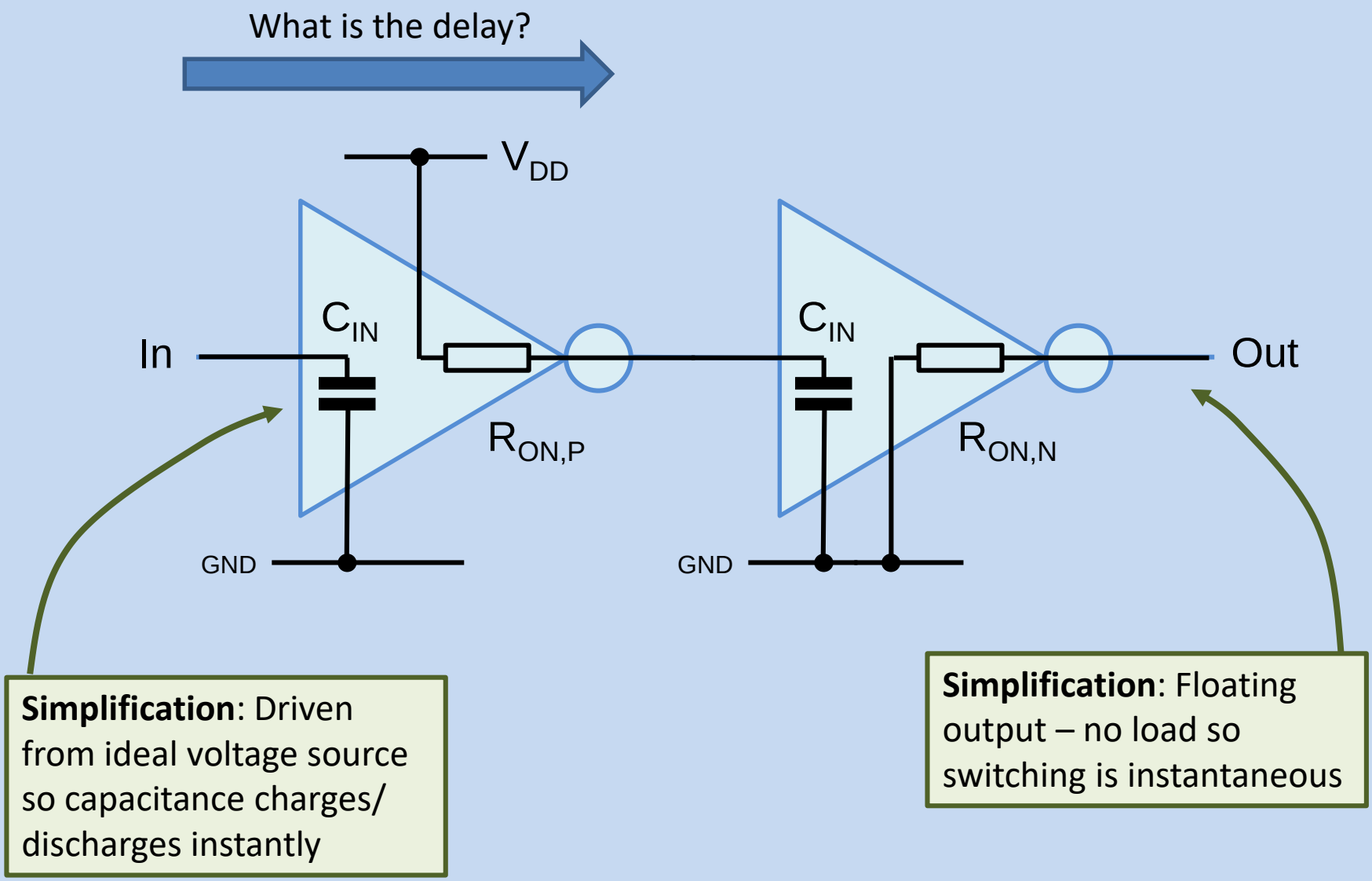
- Delay is due to time taken for the first inverter to charge or discharge the input capacitance of the second inverter (MOSFET gate capacitance)
- This depends of the amount of current the first inverter can deliver
- For a simple analysis we can assume the current depends on the first inverter's output resistance (MOSFET ON resistance of internal transistors)

Analysis of switching time – initial situation after input change

What is the delay when an 1 to 0 input change causes the middle to switch from 0 to 1?



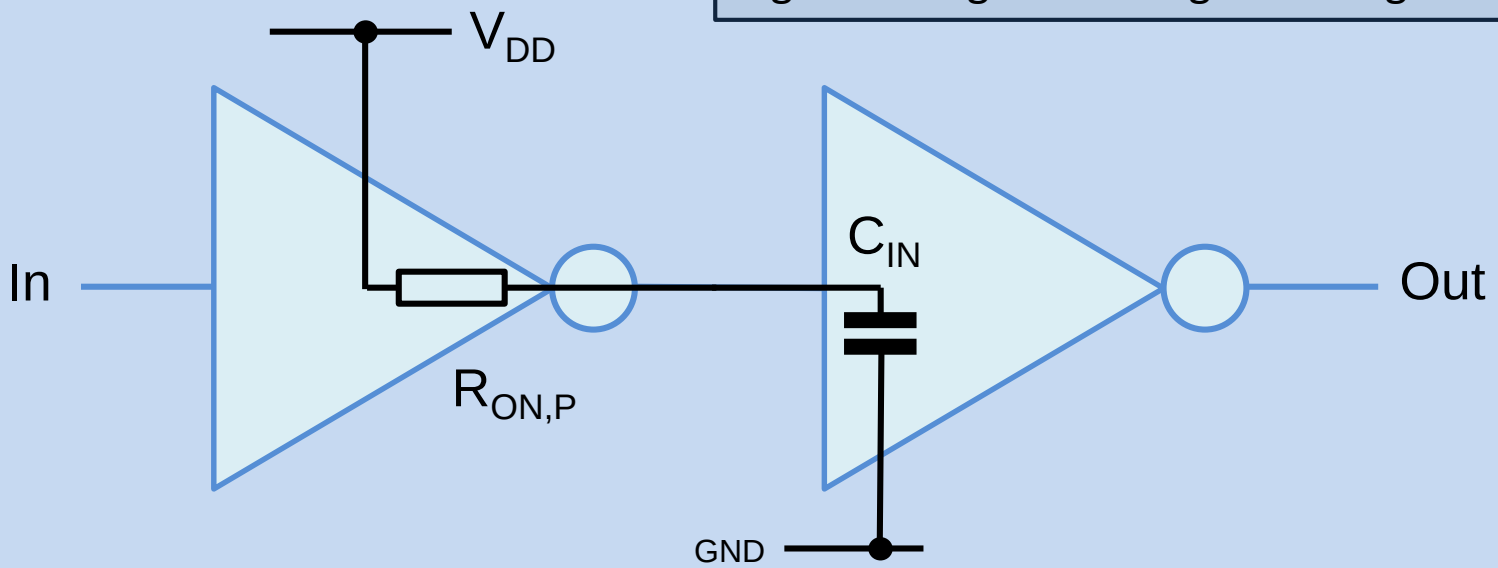
Analysis of switching time – simplifications



Analysis of switching time – analysis setup

What is the delay?

The Delay will depend on how long the capacitor takes to charge from the original logic 0 voltage to the logic 1 voltage



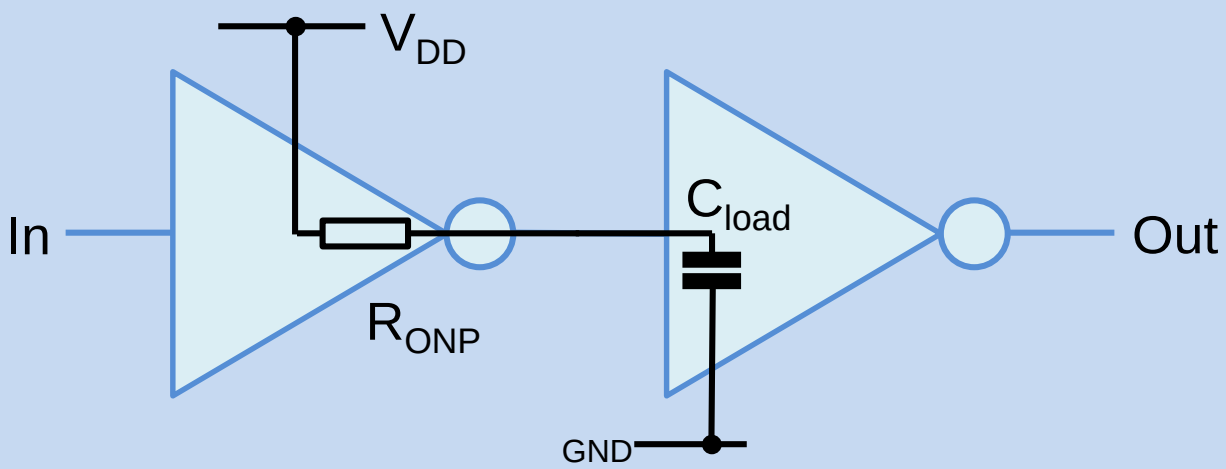
Using this simplified equivalent circuit we can estimate the delay

We calculate the delay as the time taken for the capacitor to charge through the resistor to the logic 1 input level of the second inverter

Calculating the Actual Delay Value

- Apply standard capacitance charging equation to this inverter delay
- Use R_{ONP} and $C_{load} = 2\times C_{gate}$ for the RC values
- $2\times C_{gate}$ because two MOSFET gate capacitances connected to inverter's input
- Use time change of input of first inverter as reference point t=0.
- For **propagation low-to-high**, the time, t_{PLH} , taken to reach logic high voltage V_H charging from 0V towards an applied voltage of V_{DD} is given by

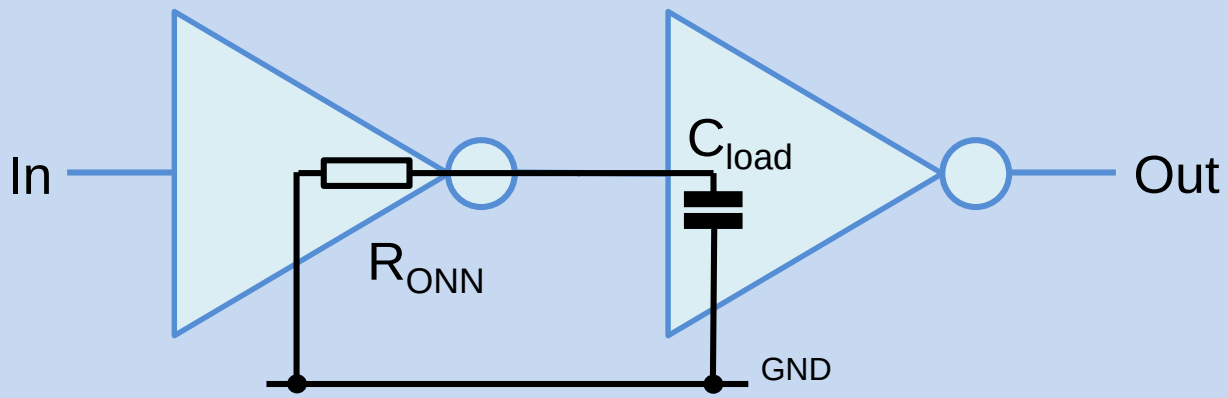
$$t_{PLH} = -R_{ONP} C_{load} \ln\left(1 - \frac{V_H}{V_{DD}}\right)$$



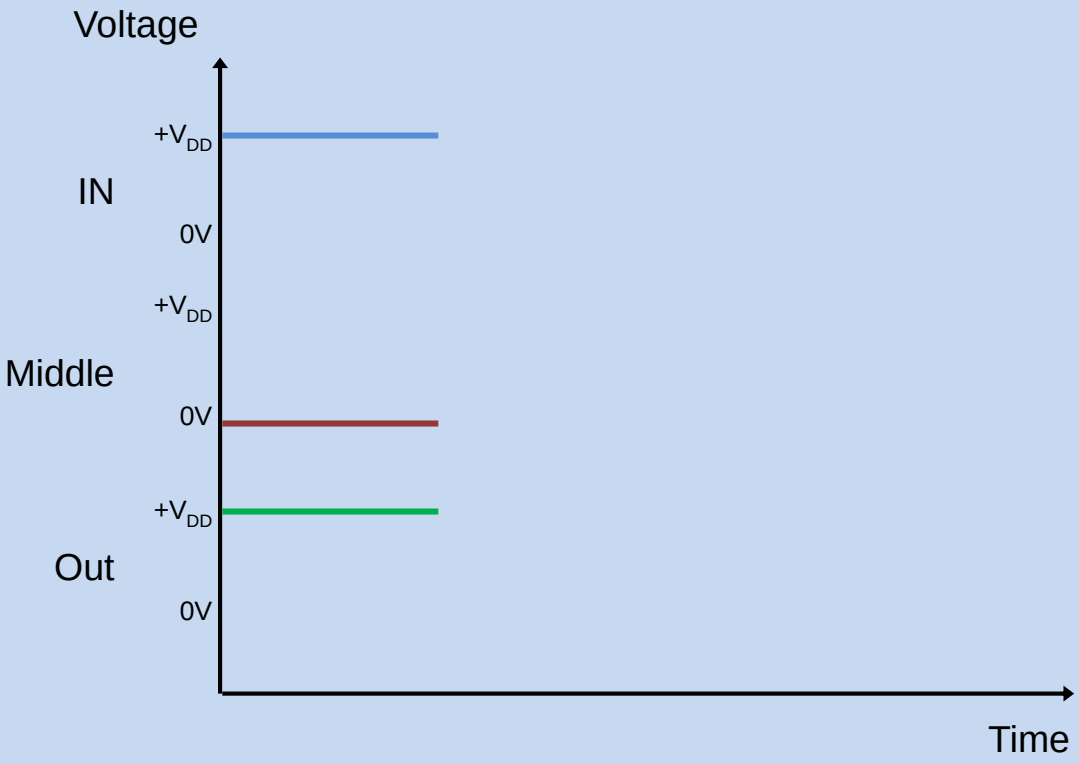
Calculating the Actual Delay Value

- For **propagation high-to-low**, the time, *t*, taken to reach logic low voltage V_L discharging from an initial voltage of V_{DD} is given by
- Again use $C_{load} = 2 \times C_{gate}$ if the load is a single inverter

$$t_{PHL} = -R_{ONN} C_{load} \ln\left(\frac{V_L}{V_{DD}}\right)$$

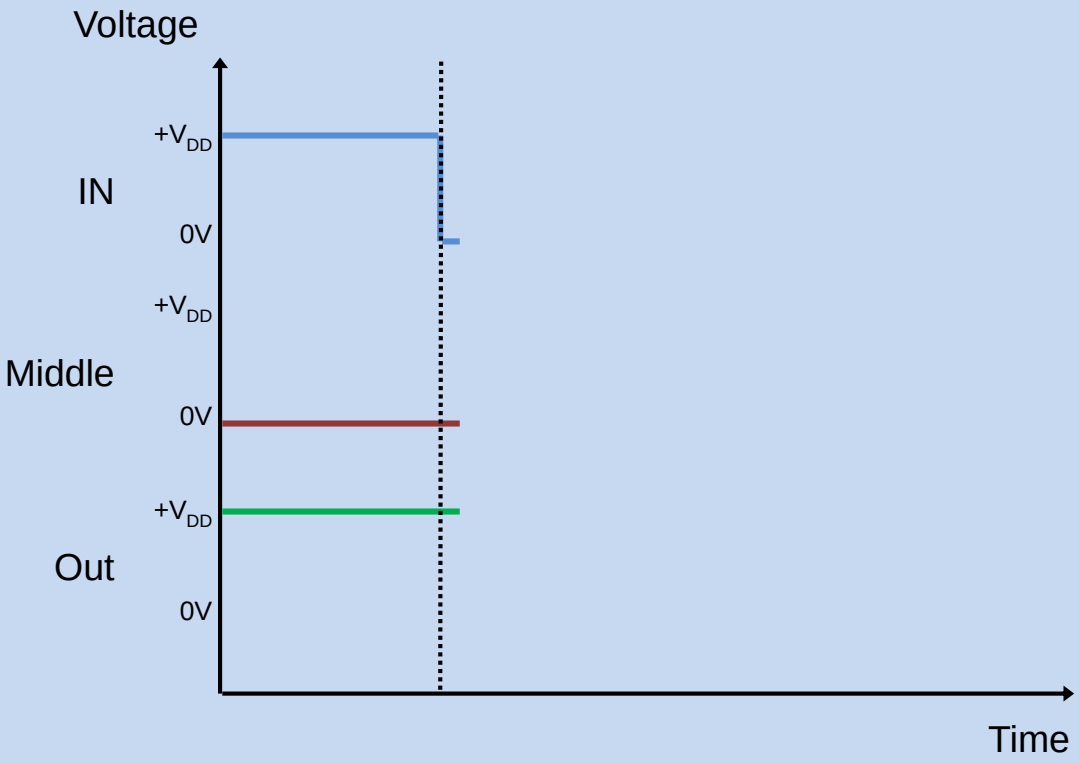


Waveforms as a function of time



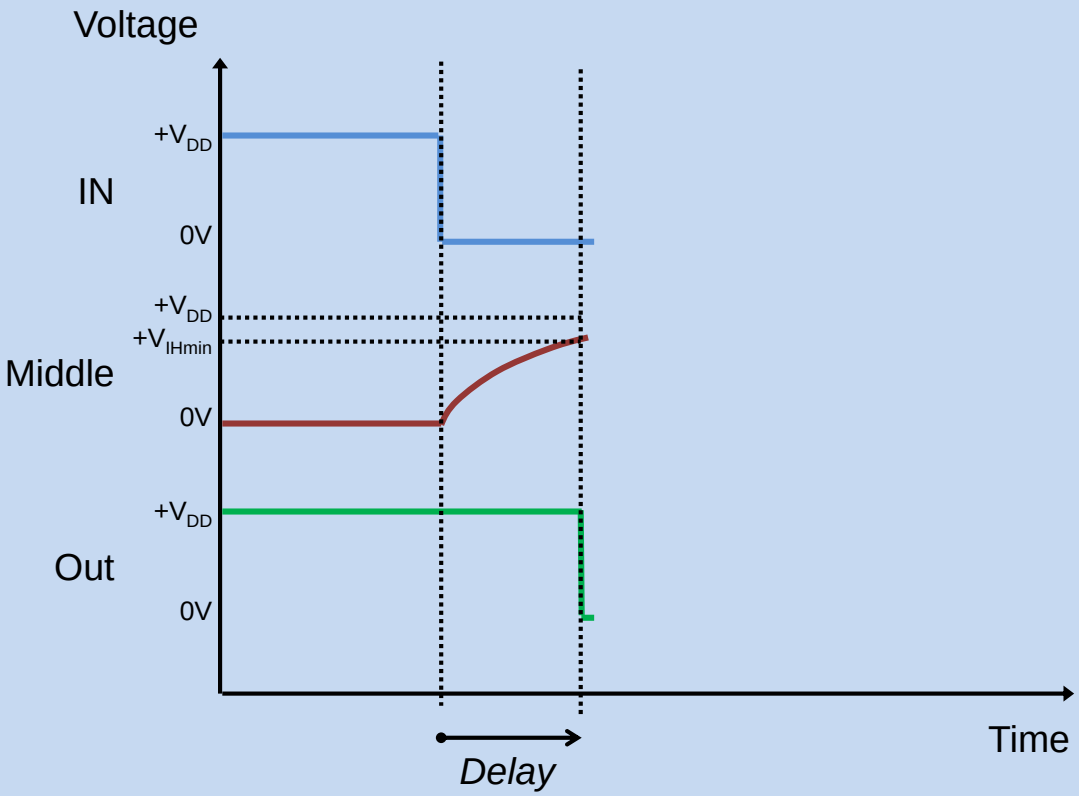
- The situation before the input changes

Waveforms as a function of time



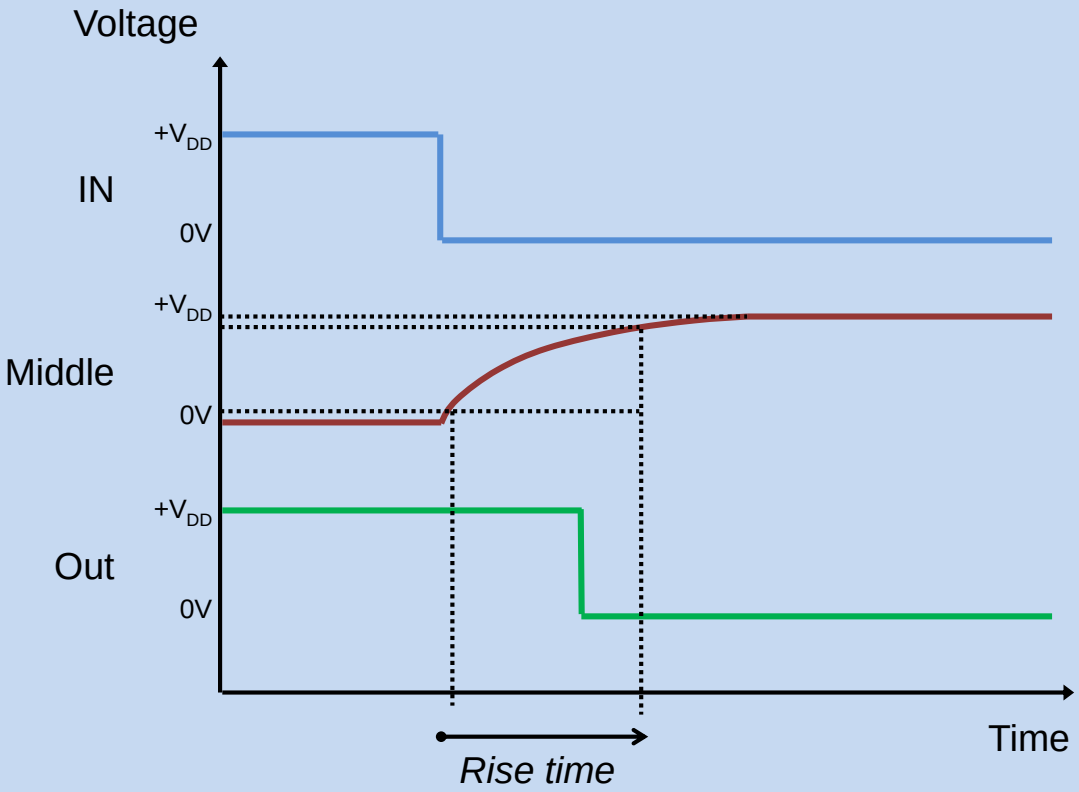
- The situation just after the input changes
- The circuit has not responded yet

Waveforms as a function of time



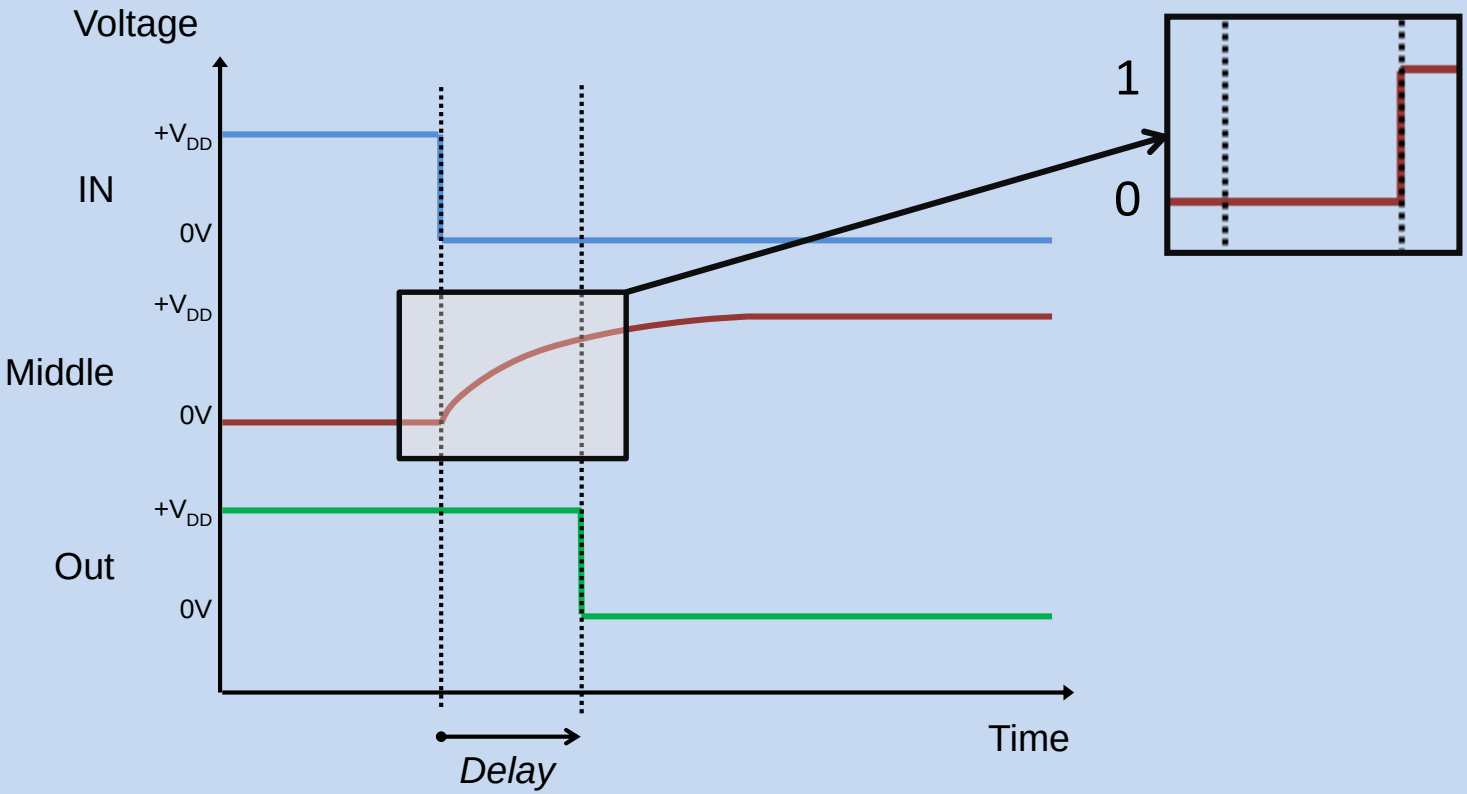
- The situation just after the second inverter switches
- We see the time **delay** for the circuit to switch in response to the input
- This is a time relationship between input and output

Waveforms as a function of time



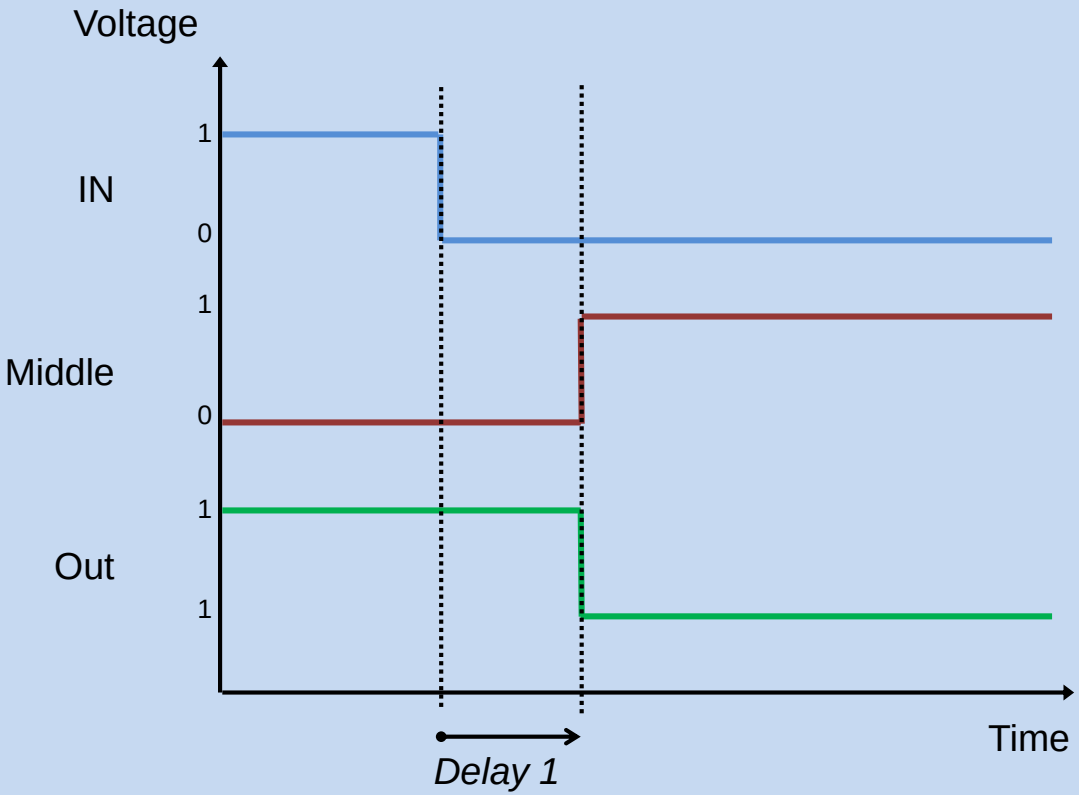
- The situation a while after the output changes
- The middle voltage continues rising towards V_{DD}
- We see the **rise time** taken for the middle signal to change from low to high

Waveforms as a function of time



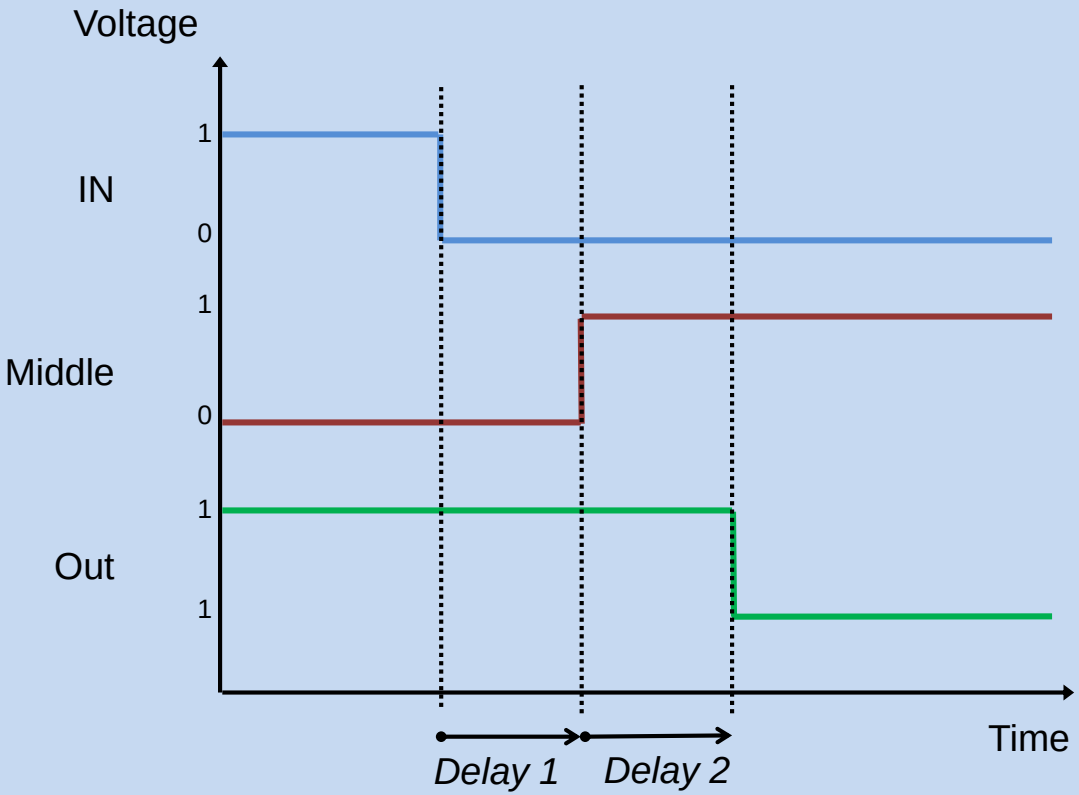
- Once we know the delay we can ignore analogue voltages and use logic 1s and 0's

Waveforms as a function of time



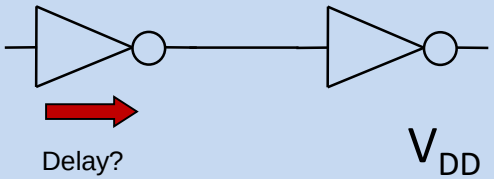
- We arrive a digital timing diagram

Waveforms as a function of time



- In this example the second inverter delay was not considered and is show as being zero
- More realistic timing showing delay for inverter 2

Example – Find delay of first inverter for input switch 1 to 0



$V_{DD} = 3.3V$

Discharge

$$t_X = -RC \ln\left(\frac{V_X}{V_0}\right)$$

Charge

$$t_X = -RC \ln\left(1 - \frac{V_X}{V_S}\right)$$

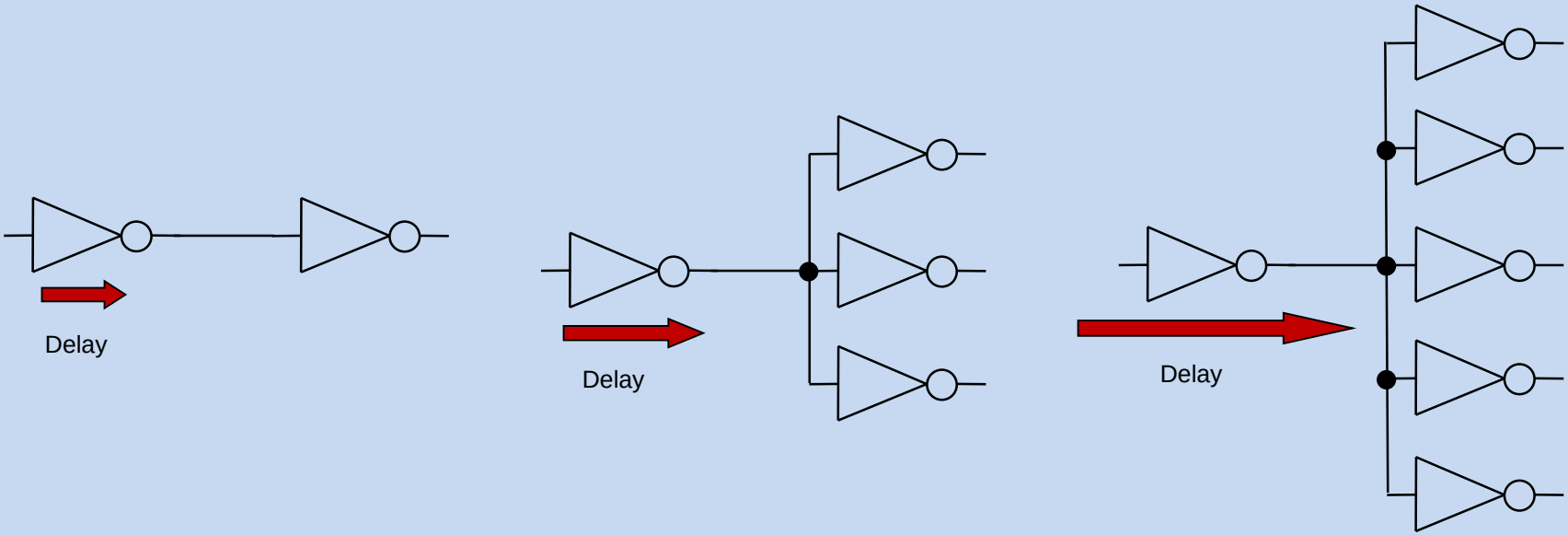
Characteristic	Value
Maximum logic 1 input voltage	3.3 V
Minimum logic 1 input voltage	2.5 V
Maximum logic 0 input voltage	0.7 V
Minimum logic 0 input voltage	0.0 V
Maximum logic 1 output voltage	3.3 V
Minimum logic 1 output voltage	3.0 V
Maximum logic 0 output voltage	0.4 V
Minimum logic 0 output voltage	0.0 V
PMOS transistor ON resistance	5.7 KΩ
NMOS transistor ON resistance	2.8 KΩ
PMOS gate capacitance	5 fF
NMOS gate capacitance	5 fF

CMOS Delay

Use of RC capacitor charging equation for delay is only approximate because

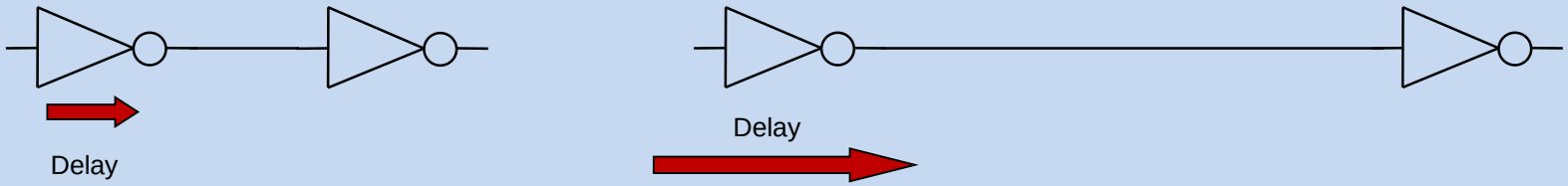
- Model of the transistor as fixed ON resistance is simplistic
- Input transition is assumed to be infinitely fast (but it isn't)
- Capacitance of the wiring (very significant on an IC) was not included.

CMOS Delay – Effect of Gate Loading



- The number of gates driven by a gate is known as the gate's **fanout**
- Increasing fanout increases the capacitance the gate has to charge/discharge
- Therefore increasing fanout increases delay

CMOS Delay – Effect of Interconnection Loading

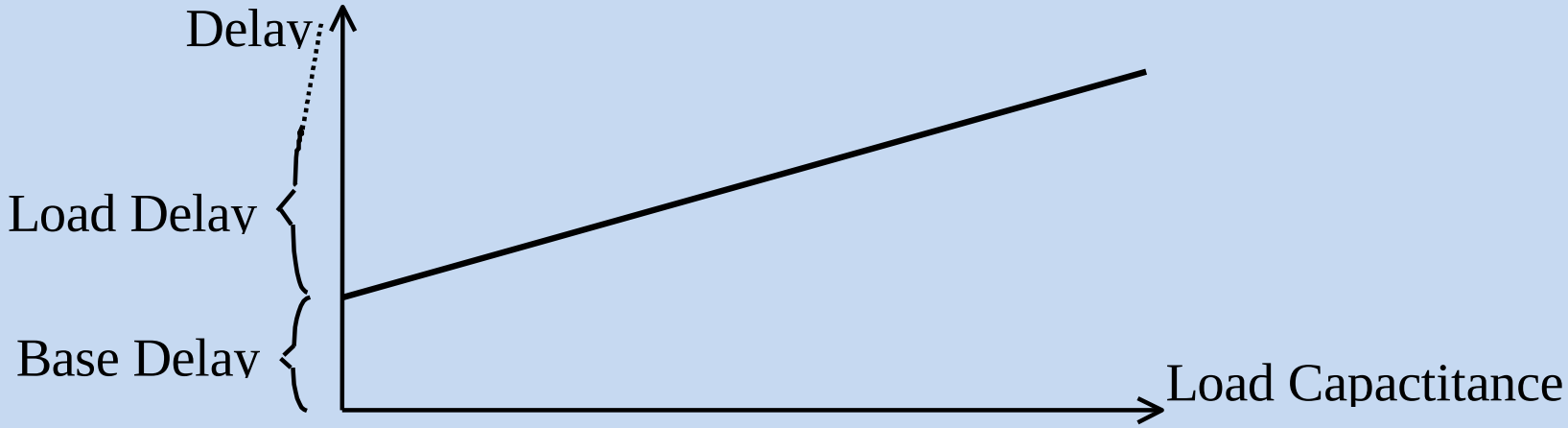


- On ICs the wires interconnecting gates have significant capacitance compared with the gate input capacitance
- Therefore increasing interconnection length increases delay
- In early digital technologies the total load capacitance was dominated by the inputs of gates
- In modern technologies the wiring capacitance dominates

CMOS Delay – Variation of Delay with Load

- An inverter with no load connected still has a propagation delay
- This is due to internal capacitances and transistor switching time
- This gives a base delay to which the load delay can be added

*Total_delay = base_delay + load_delay_factor * load_capacitance*



- CMOS delay also depends power supply voltage and temperature.