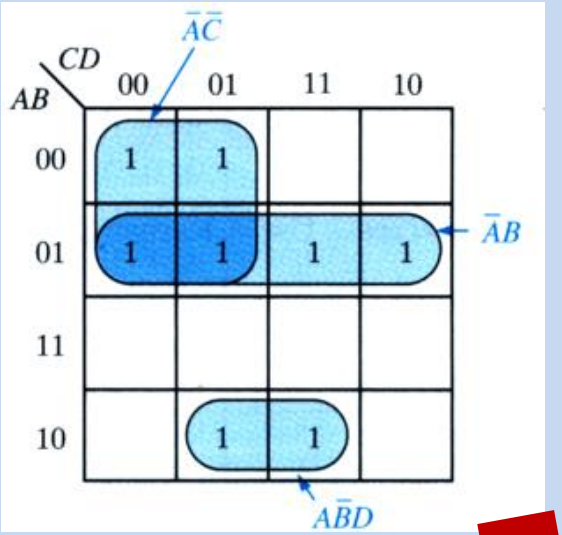
Fundamentals of Electrical and Electronic Engineering

Module 400462

Digital Electronics

Dr Ian M. Bell

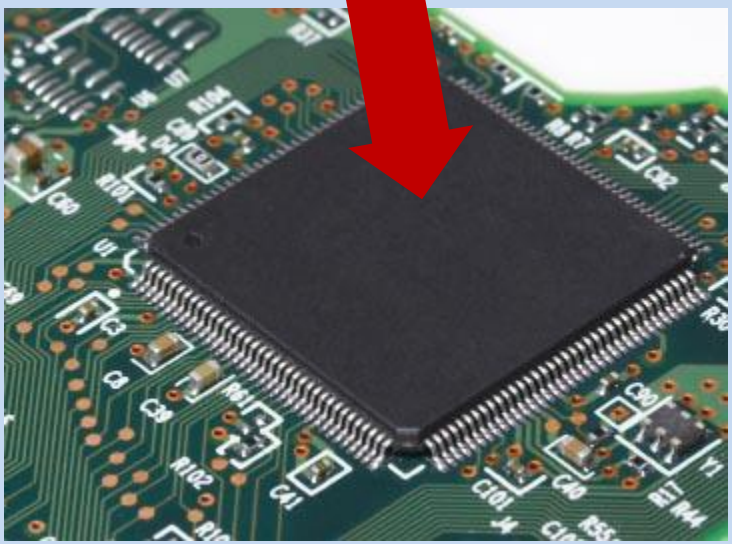
Real-World Digital Electronics



From abstract logic design to physical circuit.

What else do we need to consider

?



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Implementation Technology

- Choice of technologies for implementing a digital system
- Internal circuitry of logic gates

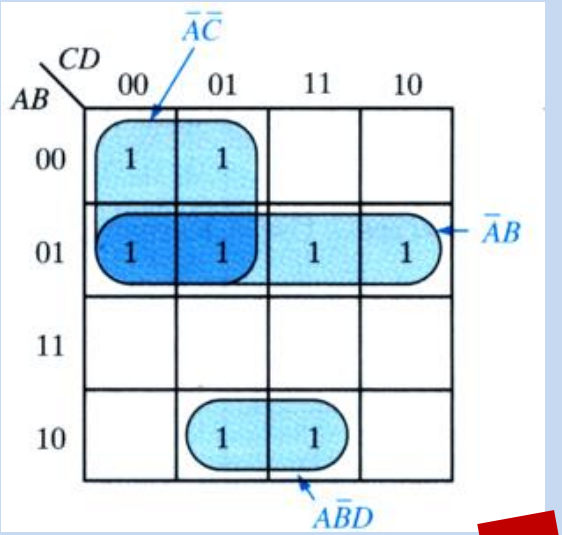
Voltage & Current

- Logic Voltages
- Noise and errors
- Supply voltages
- Power Consumption

Time

- Speed of operation
- Timing errors

Real-World Digital Electronics



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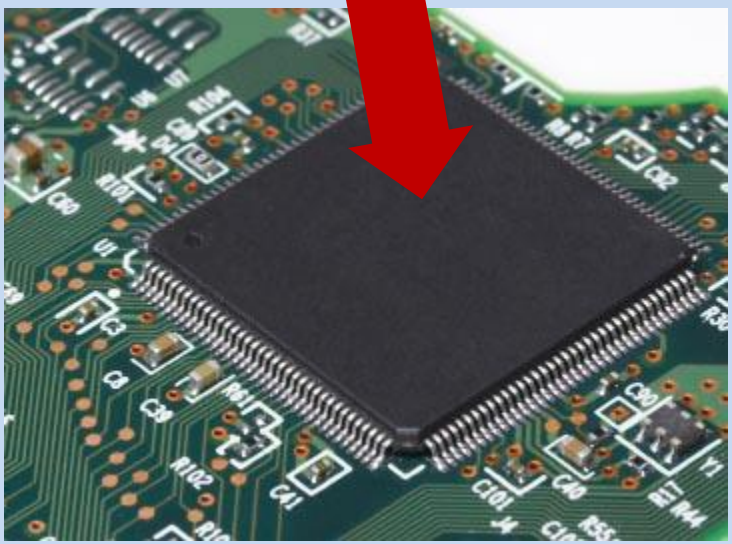

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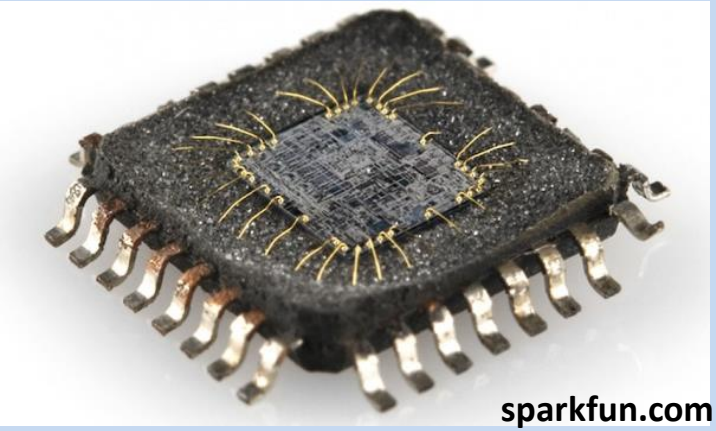
Integrated Circuits

- Digital electronics is implemented using Integrated Circuits (ICs)
  - Also know as “chips”
- ICs are made from wafers of single crystalline silicon in which structures are fabricated by processes such as
  - Adding/reacting chemicals into the silicon in selected regions
  - Depositing substances on the surface of the silicon
  - Etching to remove unwanted sections of added layers or silicon
- Multiple chips are made on one wafer
- The chips are cut out put in packages suitable for soldering onto circuit boards to create complete systems

yeint.ru

wisegeek.com


sparkfun.com

Producing Real Logic Circuits – Types of Digital IC

Options for producing a logic design as a real circuit.

1. **Discrete SSI/MSI logic** [small circuits, basic logic functions]
2. **Application-Specific Standard Product** (ASSP) [complex fixed functions]
3. **Programmable logic** [complex user-defined functions]

4. **Application-specific Integrated Circuit** (ASIC)
   [IC custom manufactured for use in a product]

Integrated circuit itself is configured at least in part by the digital circuit/system designer

Integrated circuit(s) fixed by IC manufacturer. Logic created by digital circuit/system designer using these chips

Discrete / SSI / MSI Logic

- **Discrete** – individual gates
- **SSI/MSI** Small and Medium Scale Integration
  - 1 to 100 logic gates on a chip
- Provide basic general purpose logic functions
  - Gates, flop flops, multiplexers, encoders, decoders, counters etc.
- Originally used to build large (for then) systems
- Still used for small designs/small amount of additional logic to connect other ICs ("glue logic")
- Large number of commercial Logic Families
  - New families introduced as technology developed

DEC VAX computer circuit board

computerhistory.org

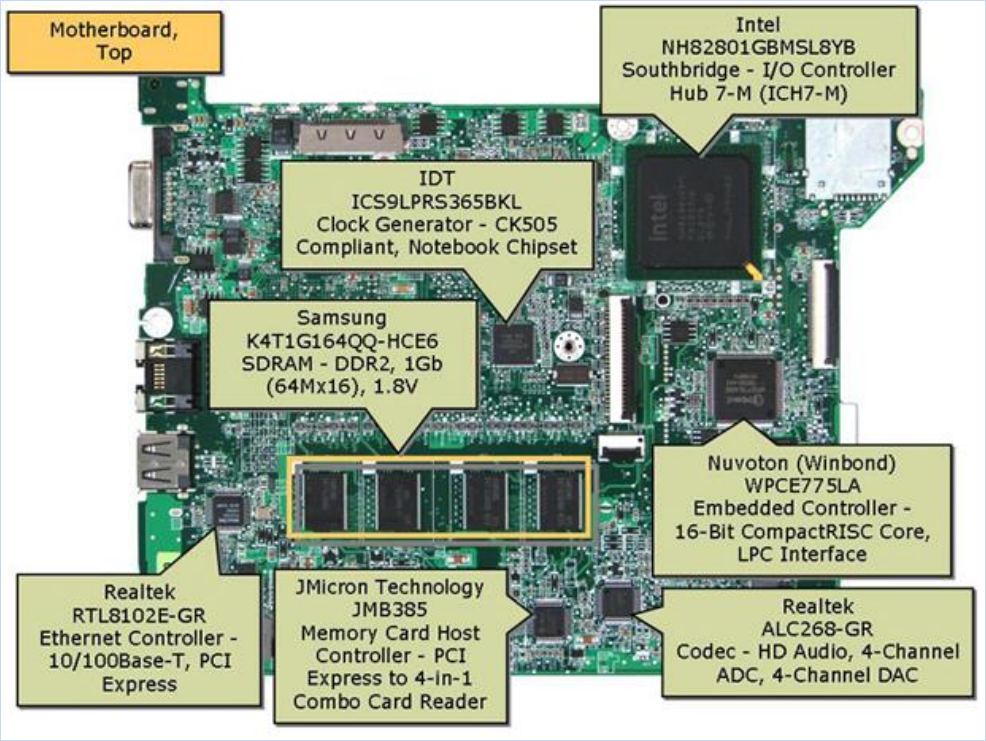
EasyN Wireless IP Camera

Showing microprocessor, Ethernet chip and 74HC259 8-bit addressable latch

www.photos-albums.com

Application-Specific Standard Product (ASSP)

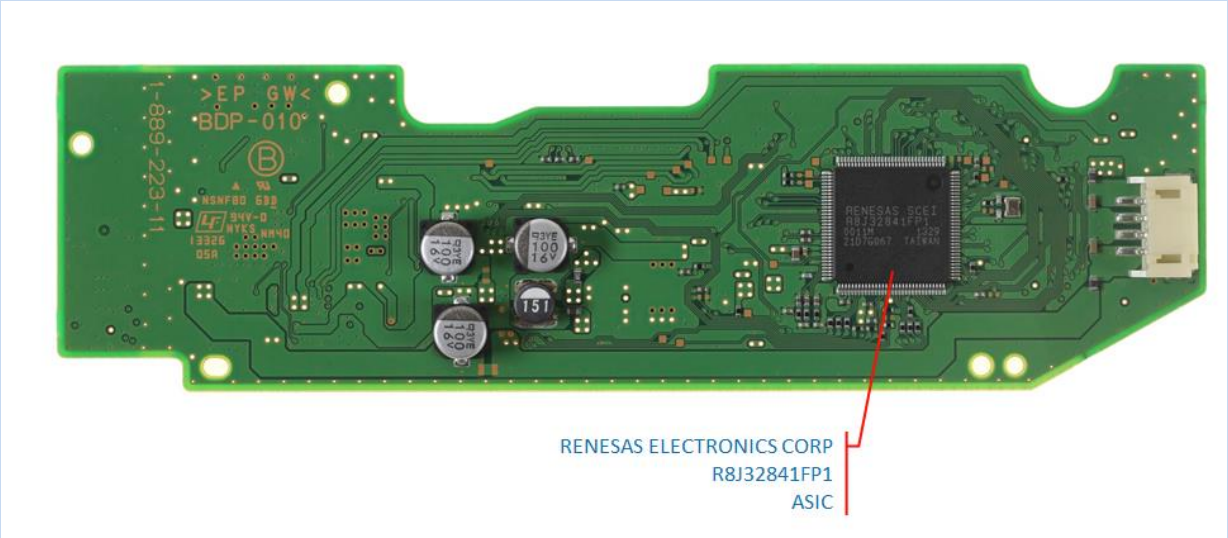
- Relatively low cost for advanced/complex functions
- Available to everyone – more difficult to provide unique capabilities
- Examples
  - Graphics Display Controllers
  - Audio Codecs/Speech Processors
  - Image Processors



Acer Aspire One ZG5 Netbook Motherboard
Various ASSP such as Ethernet Controller and Audio Codec
electronics360.globalspec.com

Application-Specific Integrated Circuit (ASIC)

- Custom-designed and manufactured integrated circuit
- High cost and time consuming development
- Difficult/expensive to change/update
- Potential for best functionality/performance/security from copying



Sony PlayStation 4– Optical Drive Controller PCB

ps3devwiki.com

Programmable logic

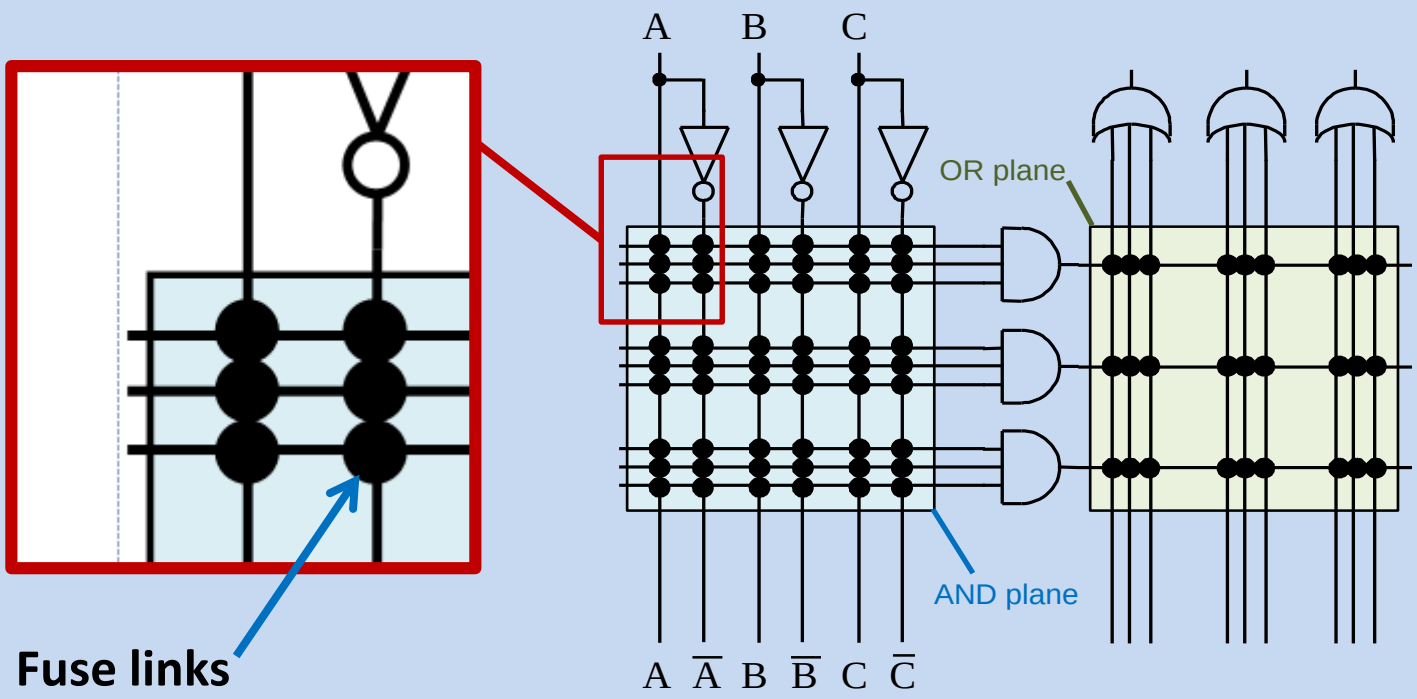
PLA	Programmable logic array
CPLD	Complex Programmable Logic Device
FPGA	Field programmable logic array

Increasing Complexity

- Enables production of custom digital logic circuits in the field (not the manufacturing stage)
- Depending on the technology used device devices may be programmable one time or many
- Here “programming” refers to configuring logic hardware to create a circuit defined by a designer – not to writing software/apps
- During development work the prototype design will usually be downloaded to the logic IC from design software on a PC
- In products blank logic IC may programmed in factory or ICs may get programmed from a non-volatile memory each time power is applied

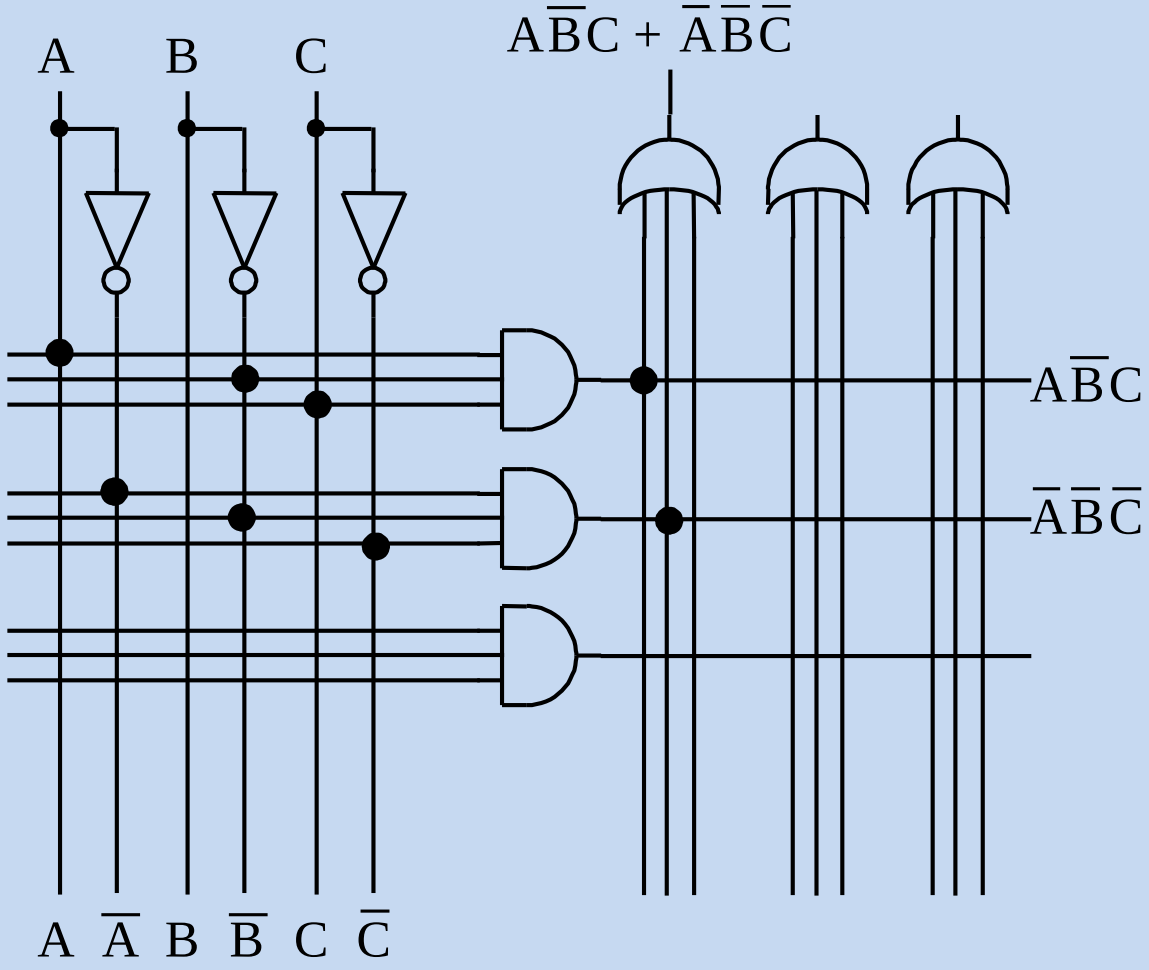
Programmable Logic Array

- Earliest form of programmable logic – dates from 1970s
- Structure of circuit directly relates to Boolean equations (e.g. Sum of Products)
- Boolean outputs may be connected to flip-flops to store data for further processing
- Once-only on-chip programming of the logic function via fuse links
- Any logic function up to the size of the chip can be obtained by blowing/leaving the appropriate link

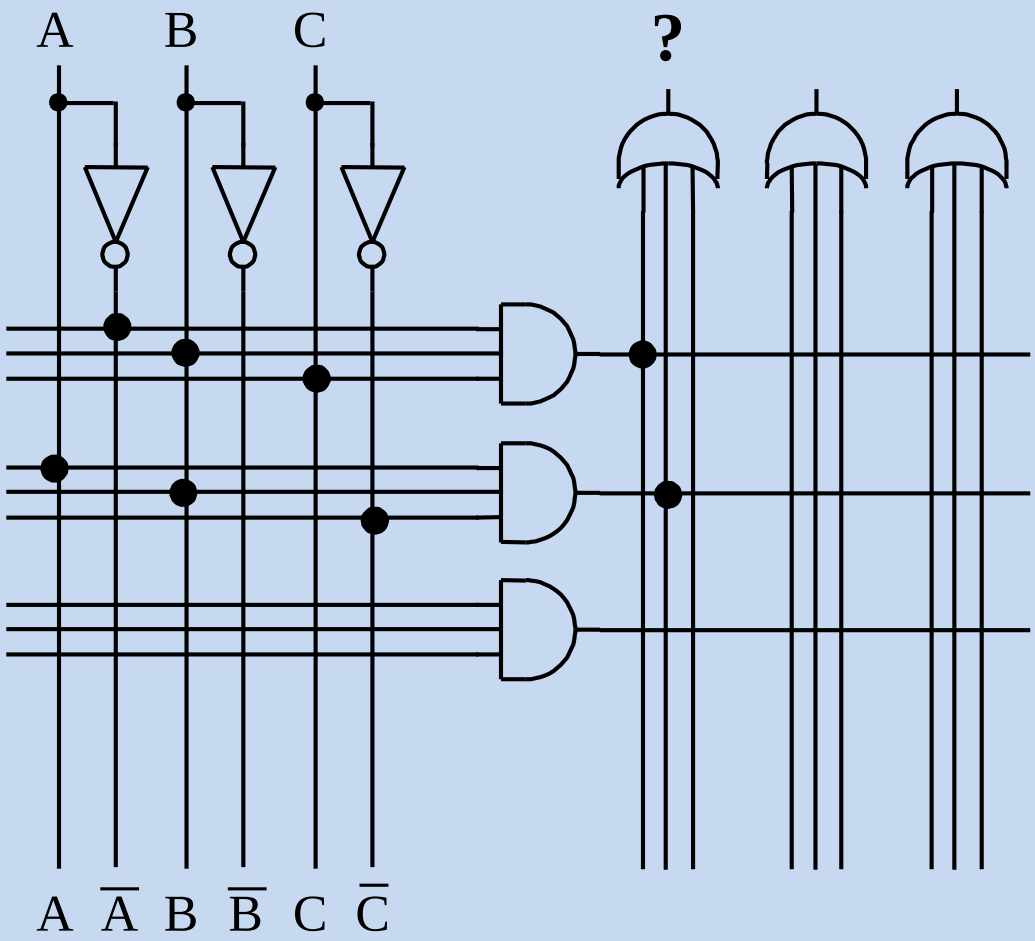


Programmable Logic Array

Example of logic function implemented using a PLA

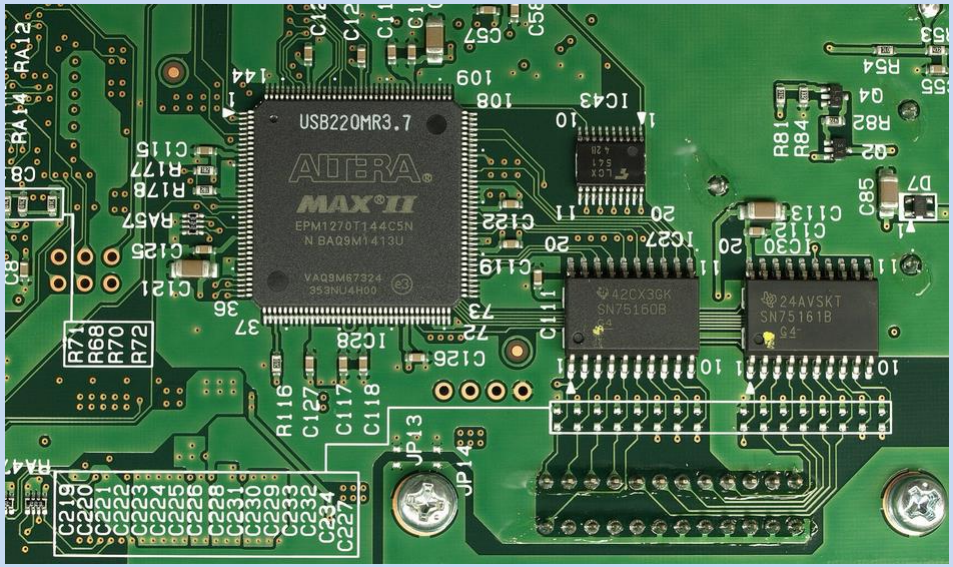


What logic function is implemented by the PLA?



CPLD - Complex Programmable Logic Device

- Like a set of PLA-like circuits (on one chip) with registers on their outputs and programmable interconnections
- Much larger circuits than PLAs (1000s to 100,000s gates)
- Typically reprogrammable
- Typically programmed in-circuit



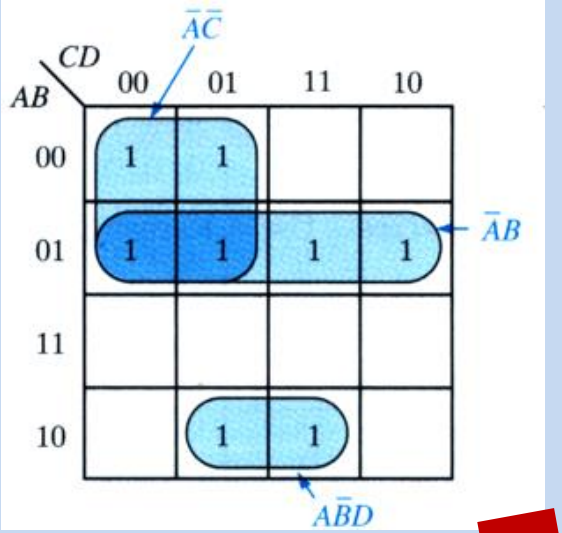
Teledyne Lecroy Wavejet Touch 354 (Iwatsu DS-5600) Oscilloscope
Altera MAX-II CPLD
eevblog.com

Field Programmable Gate Array - FPGA

- Very large amount of general purpose logic on a chip (up to tens of millions of gates)
- Logic structured in blocks
- Blocks typically contain a small programmable combination logic function, basic arithmetic function (adder) and memory (flipflops) plus circuitry to assist configuring the block's function.
- Blocks connected together by programmable wiring to form large complex digital circuits
- Designs can be produced using Hardware Description Language (HDL) code and synthesis software
- May include microprocessors and large memories as well a programmable logic

wikipedia.org

In reality there is more to worry about than just 1s and 0s



From abstract logic design to physical circuit

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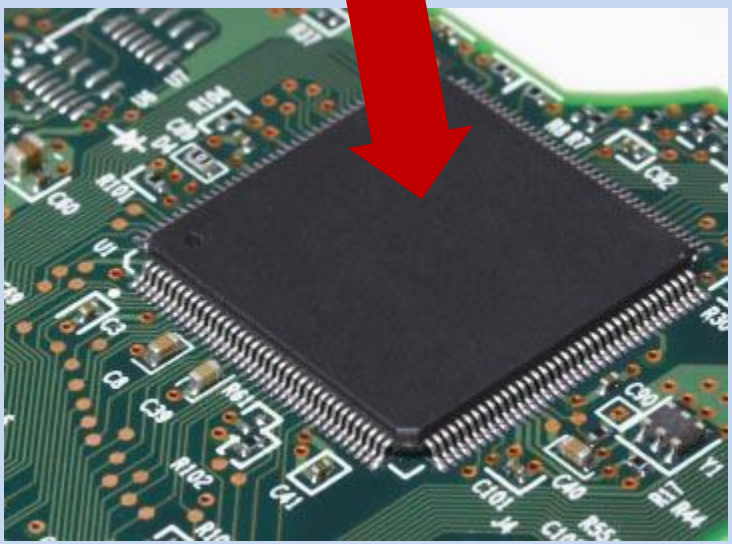

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Transistors – What logic gates are made of

Logic gates are electronic circuits build from transistors and possibly other basic electronic components

Transistors in a logic gates act as on/off switches

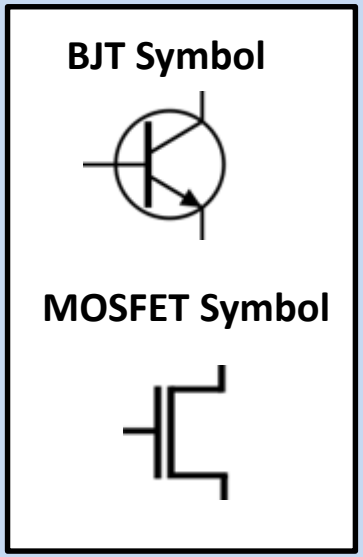
Basic types of transistor

- Bipolar Junction Transistor (**BJT**)
- Metal-Oxide-Semiconductor Field Effect Transistor (**MOSFET**)
- Junction Field Effect Transistor (**JFET**)

BJTs and MOSFETS most common in logic circuits

MOSFETs by far the most widely used

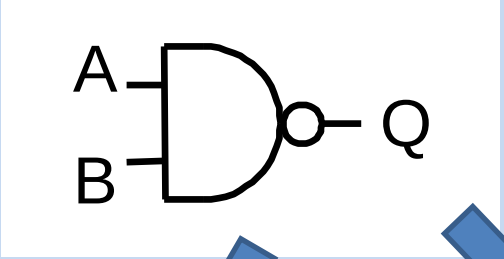
JFETs only in specialist applications



The type of “logic technology” is determined by the transistors used to implement the gate circuits.

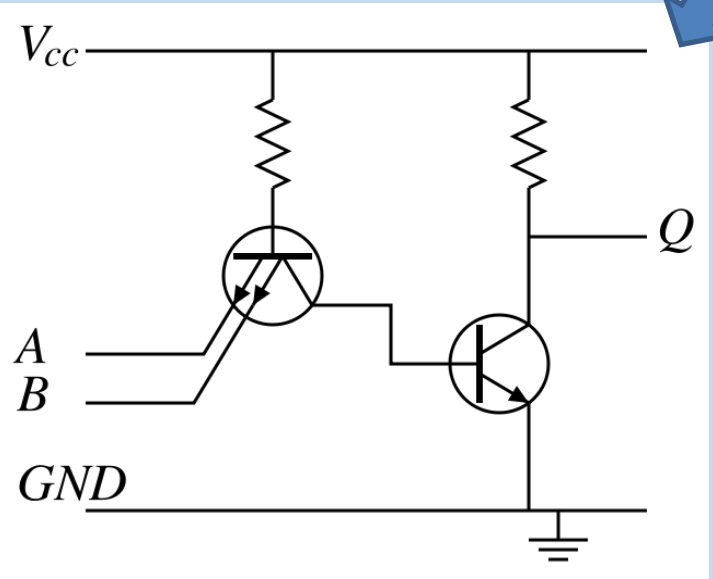
Logic Technology/Logic Family

Two key logic technologies using different transistors
TTL Transistor Transistor Logic
CMOS Complementary Metal Oxide Semiconductor



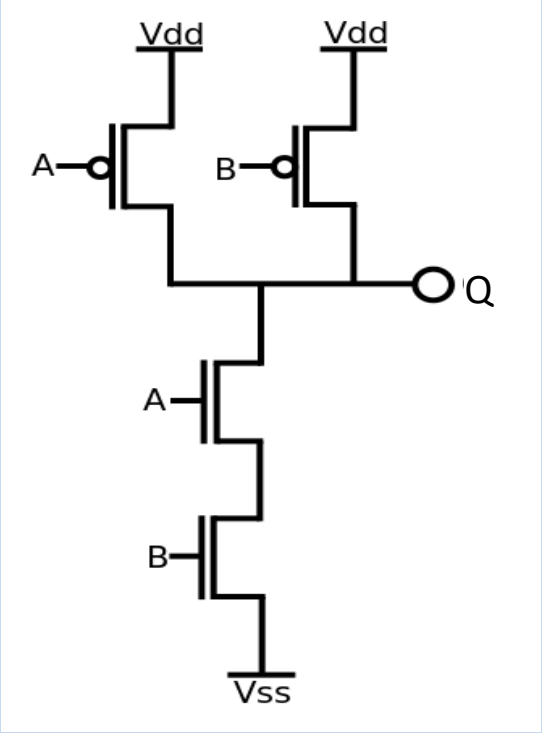
TTL

BJT transistors



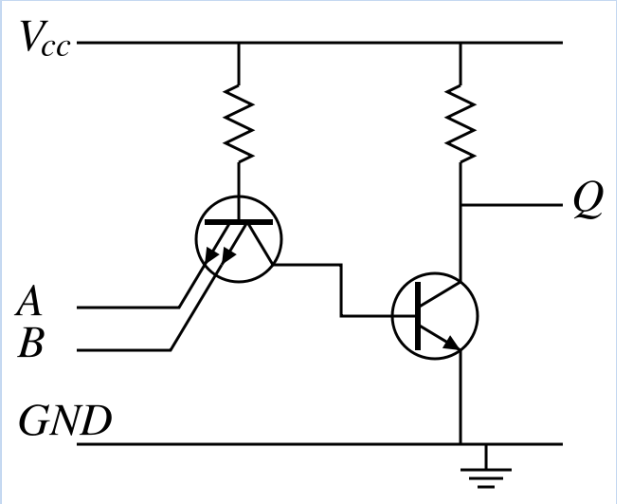
CMOS

MOSFET transistors



Commercial BJT-Based Discrete Logic families

- The first was *resistor-transistor logic* (RTL), around 1959.
- Then Diode-Transistor Logic (DTL) in 1962
- Emitter coupled logic (ECL), also 1962
- Transistor-Transistor Logic (TTL) in 1963
- Texas Instruments lower cost popular, classic 7400 IC series from 1964
- TTL and ECL prevailed and developed (e.g. becoming faster, lower power)
- TTL use was widespread, ECL more specialised (high speed)

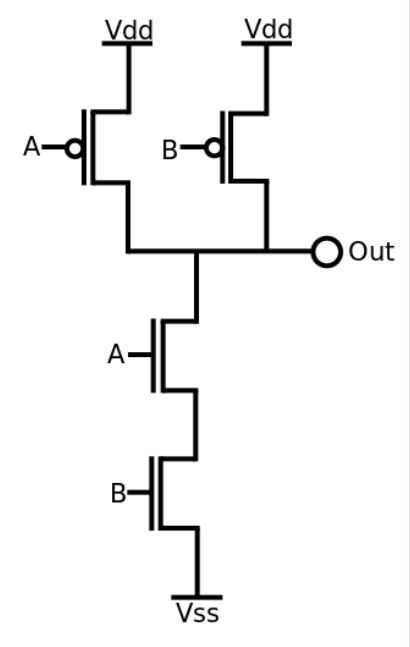


TTL

Commercial MOSFET-Based Discrete Logic Families

- Most MOS logic is now Complementary-MOS – **CMOS**
  - uses two types of MOS device which switch on opposite (complementary) logic levels (0 and 1)
- The classic CMOS logic family is the 4000 IC series
  - introduced by RCA in 1968
- CMOS versions of the 7400 series are also
  - 74HC00 and others
- MOS and bipolar transistors can be used together
  - e.g. 74ABTC series

CMOS



- CMOS technology also used now in most large integrated circuits
  - **VLSI** – Very Large Scale Integrated circuit

In this course we will mainly focus on MOSFET based circuits.

More details to follow!

Example Commercial Logic Families – Showing Technology Development

Time

7400	Standard bipolar TTL, the originals!
74LS00	Early TTL “low-power Schottky” improvement over basic 7400 series
74ALS00	Higher speed, lower power TTL than LS
74F00	High speed “Fast” TTL improvement on LS
74HCT	Direct CMOS equivalents to LSTTL. 4.5 to 5.5V supply
74AC00	CMOS, with CMOS logic levels
74ACT00	CMOS, with TTL logic levels
74FCT00	CMOS. Low power than 74F, by virtue of CMOS technology
74HC00	Basic high speed CMOS, similar to TTL, 2 to 6V supply
74LV00	CMOS 3.3V supply
74LVC00	CMOS 3.3V supply, faster, improved output over LV.

Trends:

Decreasing Supply Voltage
Increasing Speed

Example logic families from Texas Instruments (www.ti.com)

Code	Logic Family	Technology
ABT	Advanced BiCMOS Technology	BiCMOS
ABTE	Advanced BiCMOS Technology / Enhanced Transceiver Logic	BiCMOS
AC	Advanced CMOS Logic	CMOS
ACT	Advanced CMOS Logic	CMOS
AHC	Advanced High-Speed CMOS	CMOS
AHCT	Advanced High-Speed CMOS	CMOS
ALB	Advanced Low-Voltage BiCMOS	BiCMOS
ALS	Advanced Low-Power Schottky Logic	BiPolar
ALVC	Advanced Low-Voltage CMOS Technology	CMOS
ALVT	Advanced Low-Voltage CMOS Technology	BiCMOS
AS	Advanced Schottky Logic	BiPolar
AUC	Advanced Ultra-Low-Voltage CMOS Logic	CMOS
AUP	Advanced Ultra-Low-Power CMOS Logic	CMOS
AVC	Advanced Very-Low-Voltage CMOS Logic	CMOS
BCT	BiCMOS Technology	BiCMOS
CB3Q	Low-Voltage, High-Bandwidth Bus Switch Technology	CMOS
CB3T	Low-Voltage, Translator Bus Switch Technology	CMOS
CBT	Crossbar Technology	CMOS
CBT-C	CBT with Undershoot Protection	CMOS
CBTLV	Low-Voltage Crossbar Technology	CMOS
CD4000	CMOS Logic	CMOS
F	Fast Logic	BiPolar
FB	Backplane Transceiver Logic	BiCMOS
FCT	Fast CMOS Technology	CMOS
GTL	Gunning Transceiver Logic	BiCMOS
GTLP	Gunning Transceiver Logic Plus	CMOS
HC	High-Speed CMOS Logic	CMOS
HCT	High-Speed CMOS Logic	CMOS
HSTL	High-Speed Transceiver Logic	BiCMOS
JTAG	JTAG Boundary Scan Support	BiCMOS
LS	Low-Power Schottky Logic	BiPolar
LV-A	Low-Voltage CMOS Technology	CMOS
LV-AT	Low-Voltage CMOS Technology	CMOS
LVC	Low-Voltage CMOS Technology	CMOS
LVT	Low-Voltage BiCMOS Technology	BiCMOS
PCA	Inter Integrated Circuit	CMOS
PCF	Inter Integrated Circuit	CMOS
S	Schottky Logic	BiPolar
SSTL	Stub Series Terminated Logic	BiCMOS
SSTV	Stub Series Terminated Low-Voltage Logic	CMOS
TCA	Inter Integrated Circuit	CMOS
TS	TI Switch	CMOS
TTL	Transistor-Transistor Logic	BiPolar
TVC	Translation Voltage Clamp	CMOS
VME	VME Bus Products	CMOS

CMOS vs. TTL Comparison

CMOS (e.g. 4000 series)

- Are susceptible to damage by static electricity (so handle with care)
- 4000 series: 3V to 15V supplies (other series require different voltages)
- Behave unpredictably if inputs are left unconnected
- May have very low power consumption when not switching (static)
- Analogue signal switching and routing functions available

TTL (e.g. 74LS series)

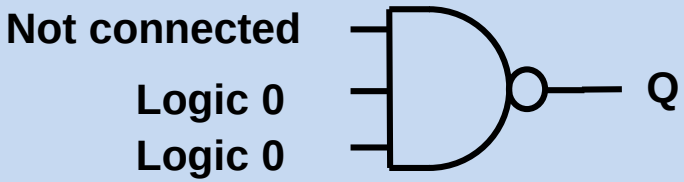
- Not static sensitive.
- Must have a supply of 5V (+/- 0.5V)
- Inputs behave as logic 1 when left floating
- Relatively high (static) power consumption
- No analogue switch functions.

Be aware behaviour/requirements of the different logic families

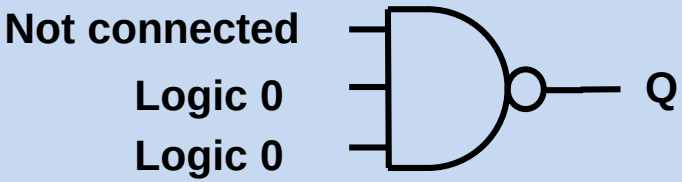
“TTL” is sometimes used to refer to use of TTL compatible voltage levels even if a system is not implemented with this technology (e.g. “TTL inputs”)

One input of the gate is not needed so left unconnected
What is the output (Q) in each case?

CMOS logic gate



TTL logic gate



In general it is bad practice to leave any unused logic input floating (not connected)

Connect to an appropriate fixed logic level unless the datasheet specifies otherwise

Integrated Circuit Identification Codes (Example)

CD	4011	B	E	XX	E4
1	2	3	4	5	6

Part	Description	Examples
1	Prefix - Designates the manufacturer	CD
2	Type - The logic function, up to five digits	4016 4049
3	Supply Voltage	A – 12 V Maximum B – 18 V Maximum UB – 18 V Maximum, Unbuffered
4	Package format	E – Plastic Dual-In-Line Package (DIP) F – Ceramic DIP M – Plastic Surface-Mount Small-Outline Integrated Circuit (SOIC) There are many more of these.
5	High–Reliability Screening. This code indicates compliance with MIL standards for military products only.	
6	RoHS and Green Status	Codes to indicate conformance to Lead-Fee and other environmental standards

Data Sheets

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised March 2002

CD4001BC/CD4011BC
Quad 2-Input NOR Buffered B Series Gate • Quad 2-Input NAND Buffered B Series Gate

General Description

The CD4001BC and CD4011BC quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL:
  Fan out of 2 driving 74L compatibility: or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 µA at 15V over full temperature range

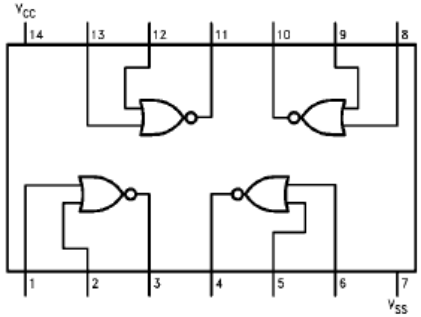
Ordering Code:

Order Number	Package Number	Package Description
CD4001BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4001BCSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4001BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4011BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4011BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

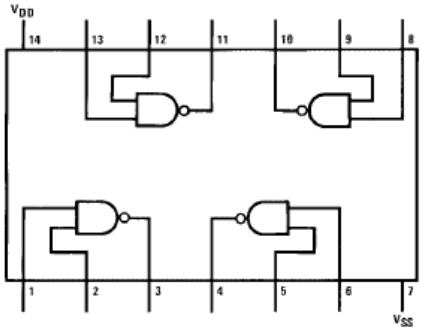
Connection Diagrams

Pin Assignments for DIP, SOIC and SOP
CD4001BC



Top View

Pin Assignments for DIP and SOIC
CD4011BC



Top View

CD4001BC/CD4011BC Quad 2-Input NOR Buffered B Series Gate • Quad 2-Input NAND Buffered B Ser

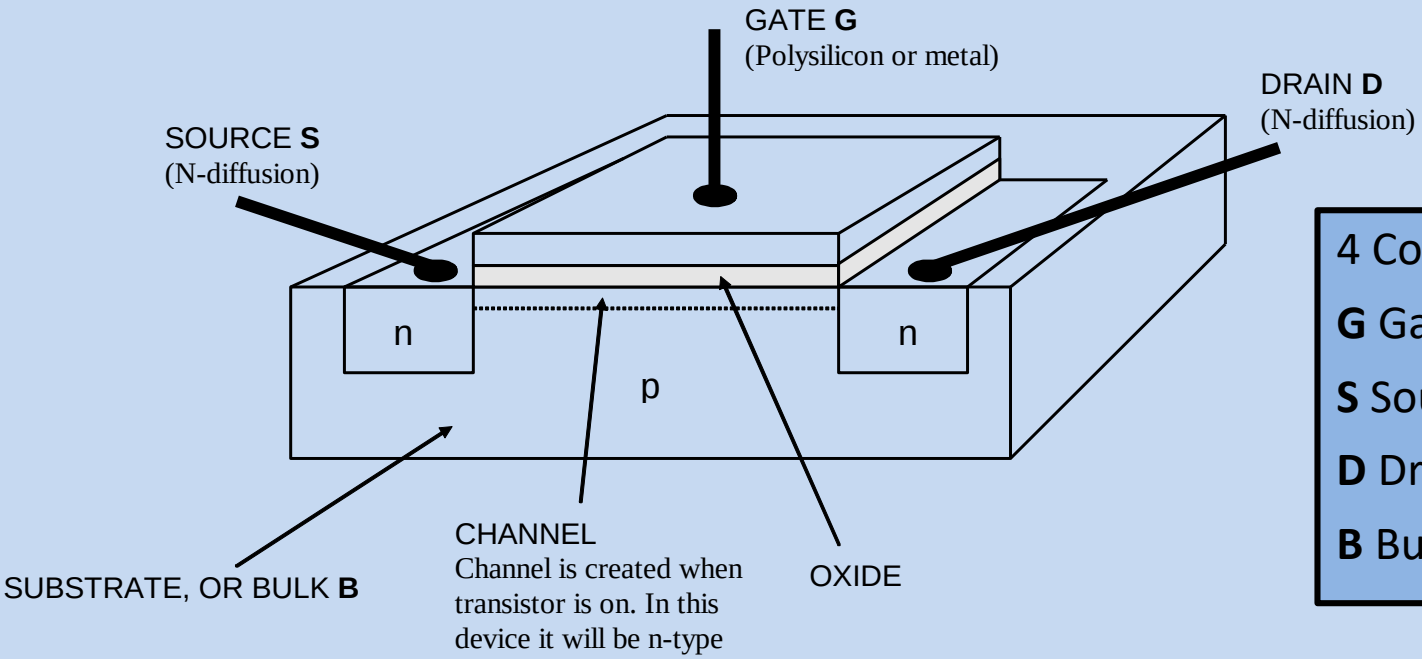
Provided by IC manufacturer

Available on manufacturers' web sites (as PDF files).

Provide

- Detailed description of function/operation
- Connection details ("pinouts")
- Performance information (e.g. speed)
- Operating conditions (e.g. supply voltage)

Simplified Structure of an N-Channel MOSFET Transistor



4 Connections:

G Gate

S Source

D Drain

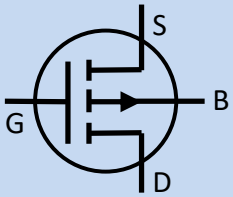
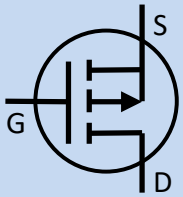
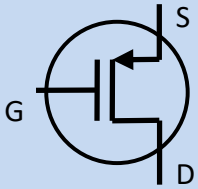
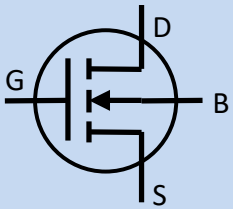
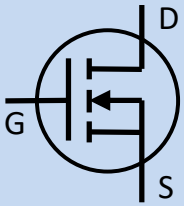
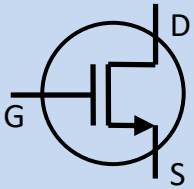
B Bulk or Substrate

The **MOS** in **MOSFET** comes from the physical structure of the device – the 3 layers:

- ❑ "Metal" **Gate** terminal (control)
- ❑ "Oxide" Insulator (isolates gate from channel)
- ❑ "Semiconductor" Channel (switch conductor)
  – Connects **Source** and **Drain** terminals when transistor is ON

FET – "Field Effect" refers to the fact that the gate is insulated from the rest of the device and controls it through an electrical field, not via current flow.

MOSFET Circuit Symbols

	Full Symbol	Full Symbol (bulk connected to source)	Simplified Symbol
P			
N			

The “Bulk”, which is the bulk semiconductor in which the transistor is formed, is often directly shorted to the source

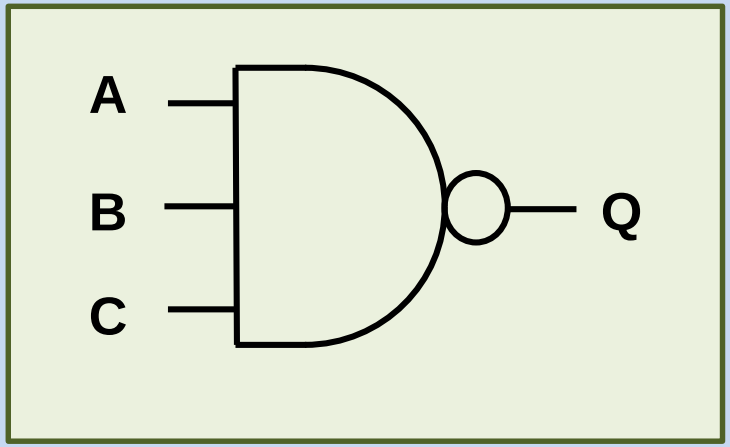
We get a three terminal rather than four terminal device

The MOSFET symbol simplified to reflect this

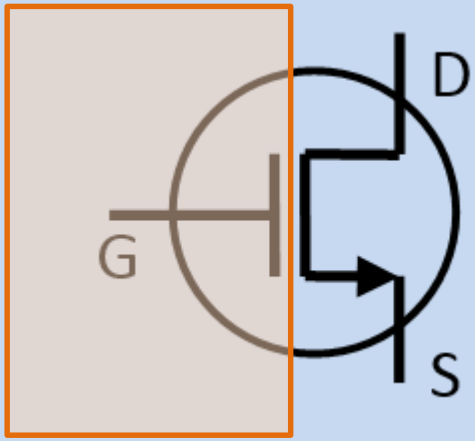
Gates - Don’t get confused

We are using the word **gate** for two different things

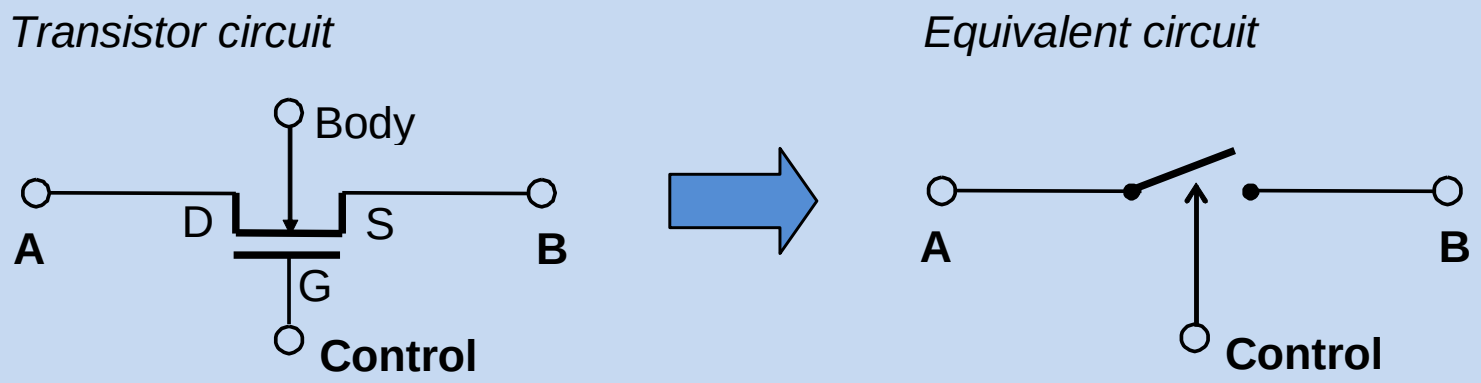
Logic gate



MOSFET gate terminal

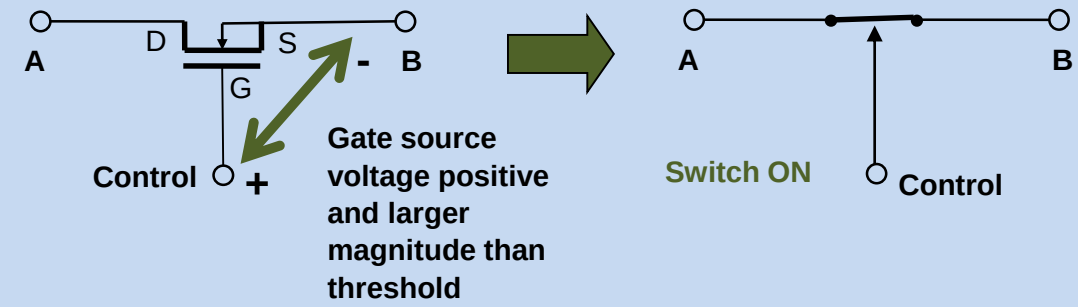


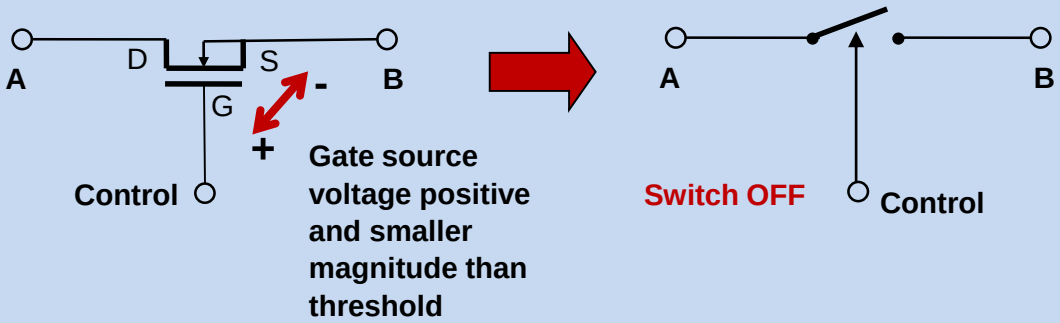
Building Logic Gates - The transistor as a switch



- The voltage between the Gate and Source terminals V_{GS} determines if the MOSFET switch is ON or OFF
- V_{GS} is the voltage at the Gate terminal as measured from Source terminal
- If the magnitude of V_{GS} is greater than a certain voltage, the threshold voltage, V_T the transistor switch will be ON
- The polarity of V_{GS} required to switch the transistor ON depends on the type of transistor
- N channel MOSFET (NMOS) – V_{GS} positive to turn on
- P channel MOSFET (PMOS) – V_{GS} negative to turn on

NMOS Switch



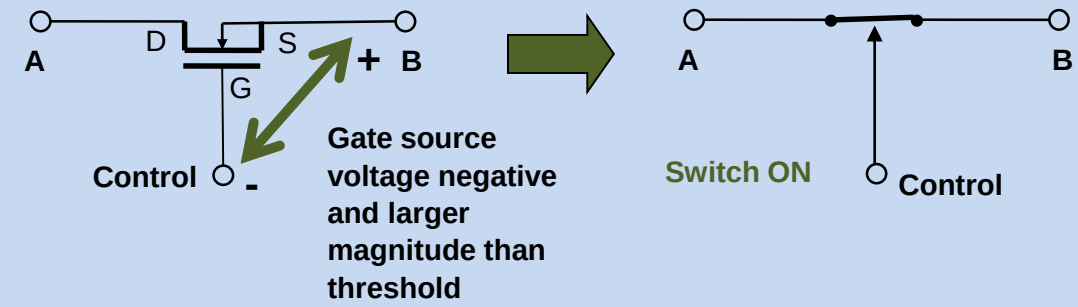


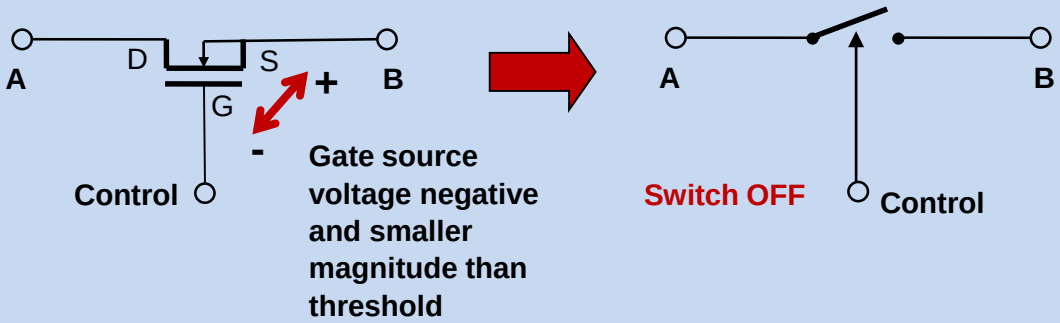
The NMOS transistor requires a positive V_{GS} larger the threshold to switch on

Example (with threshold of 1V)

- Source at 0V (ground), Gate at +5V (supply voltage) → V_{GS} = 5V → switch ON
- Source at 0V (ground), Gate at 0V (ground) → V_{GS} = 0V → switch OFF

PMOS Switch



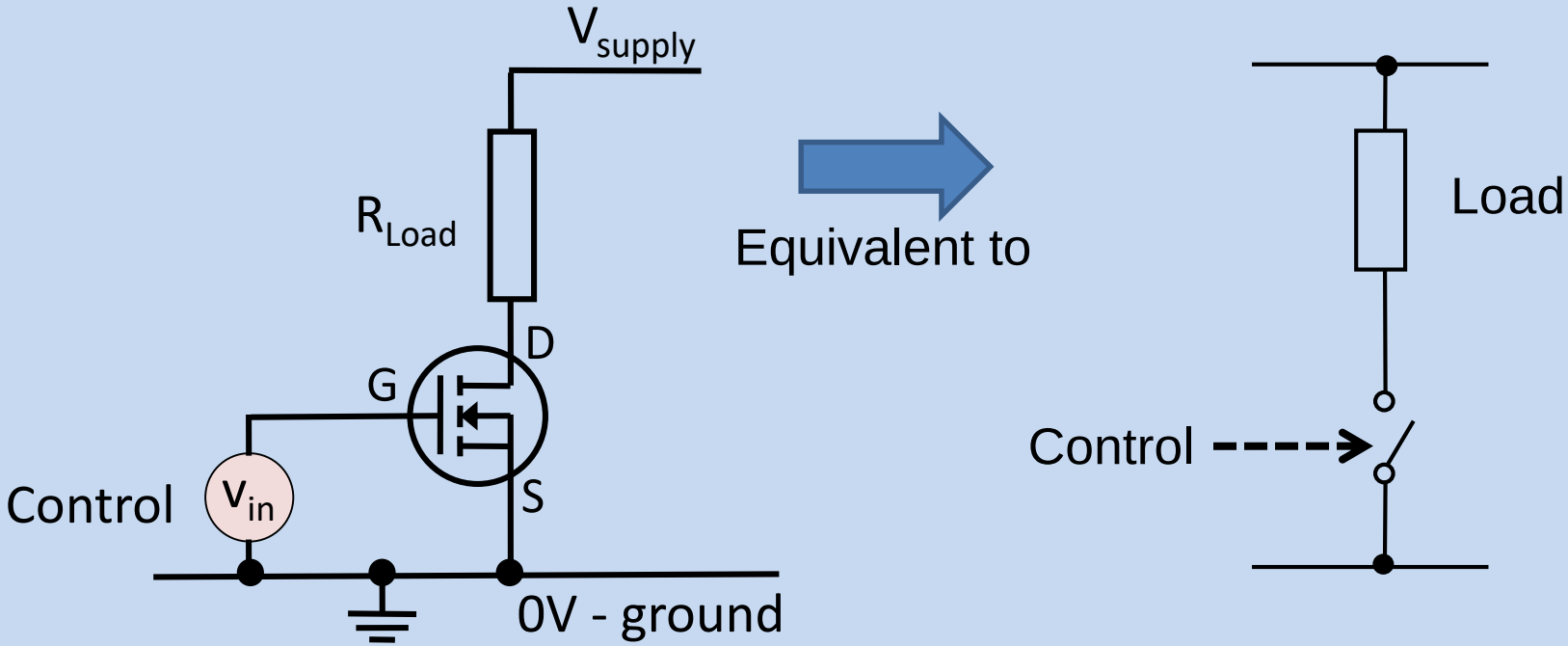


The PMOS transistor requires a negative V_{GS} larger the threshold to switch on

Example (with threshold of -1V)

- Source at +5V (supply voltage), Gate at 0V (ground), → V_{GS} = -5V → switch ON
- Source at +5V (supply voltage), +5V (supply voltage) → V_{GS} = 0V → switch OFF

NMOS switch circuit

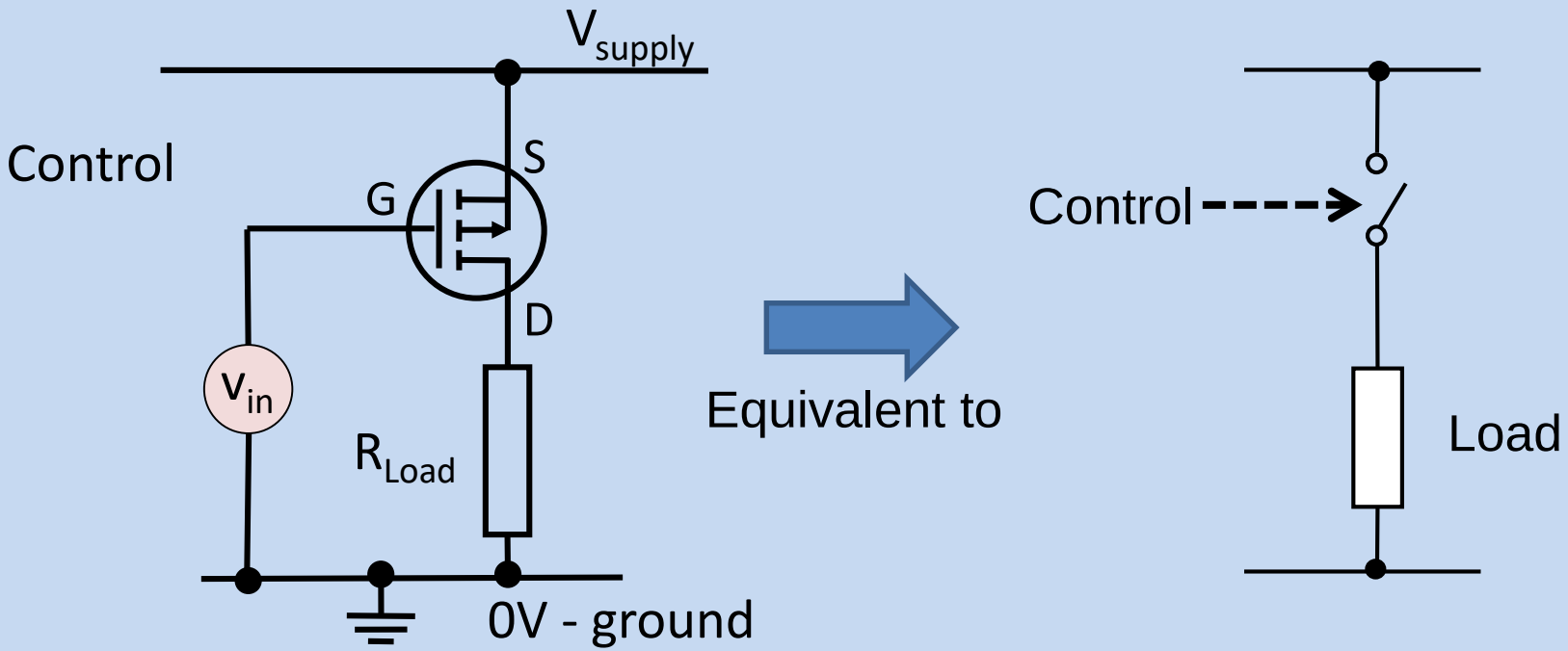


The NMOS transistor is switched ON by a **positive** gate-source voltage

Current will flow in the load if the gate-source voltage is larger than the threshold (Assume $V_{supply} > V_T$)

- $V_{in} = V_{supply}$ $V_{GS} = V_{supply}$ Switch **ON**
- $V_{in} = 0V$ $V_{GS} = 0V$ Switch **OFF**

PMOS switch circuit



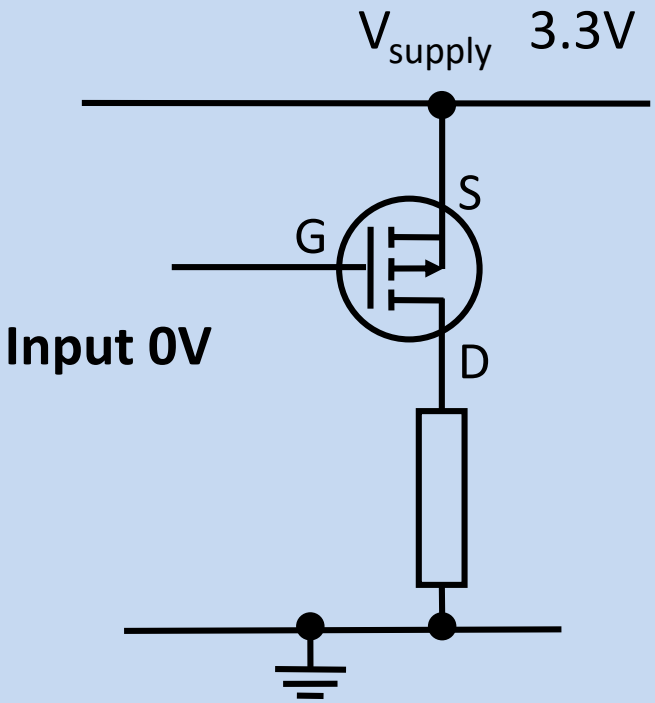
The PMOS transistor is switched ON by a **negative** gate-source voltage

As the source is connected to the positive power supply voltage, applying 0V at the gate will result in a *negative* V_{GS} and switch the transistor ON

Current will flow in the load if the gate-source voltage magnitude is larger than the threshold (Assume $V_{supply} > V_T$)

- $V_{in} = V_{supply}$ $V_{GS} = 0V$ Switch **OFF**
- $V_{in} = 0V$ $V_{GS} = -V_{supply}$ Switch **ON**

Is the switch ON or OFF ?



MOSFET switch logic

Represent logical 0 and 1 as follows

- V_{supply} Logic 1
- *0V* Logic 0

Typical power supply voltages for logic chips

- *5V*
- *3.3 V*
- *2.5 V*
- *1.8V*

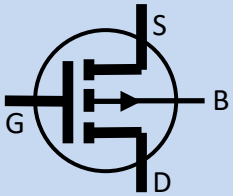
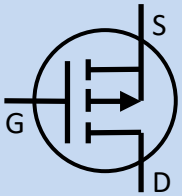
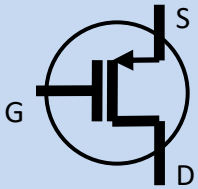
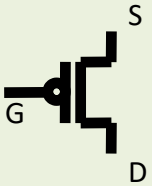
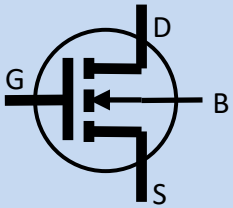
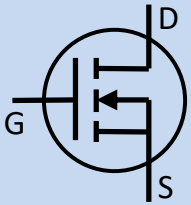
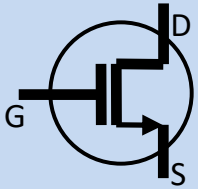
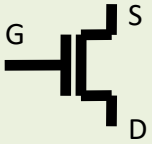
NMOS

- $V_{in} = V_{supply}$ Switch ON **Logic 1 – Switch ON**
- $V_{in} = 0V$ Switch OFF **Logic 0 – Switch OFF**

PMOS

- $V_{in} = V_{supply}$ Switch OFF **Logic 1 – Switch OFF**
- $V_{in} = 0V$ Switch ON **Logic 0 – Switch ON**

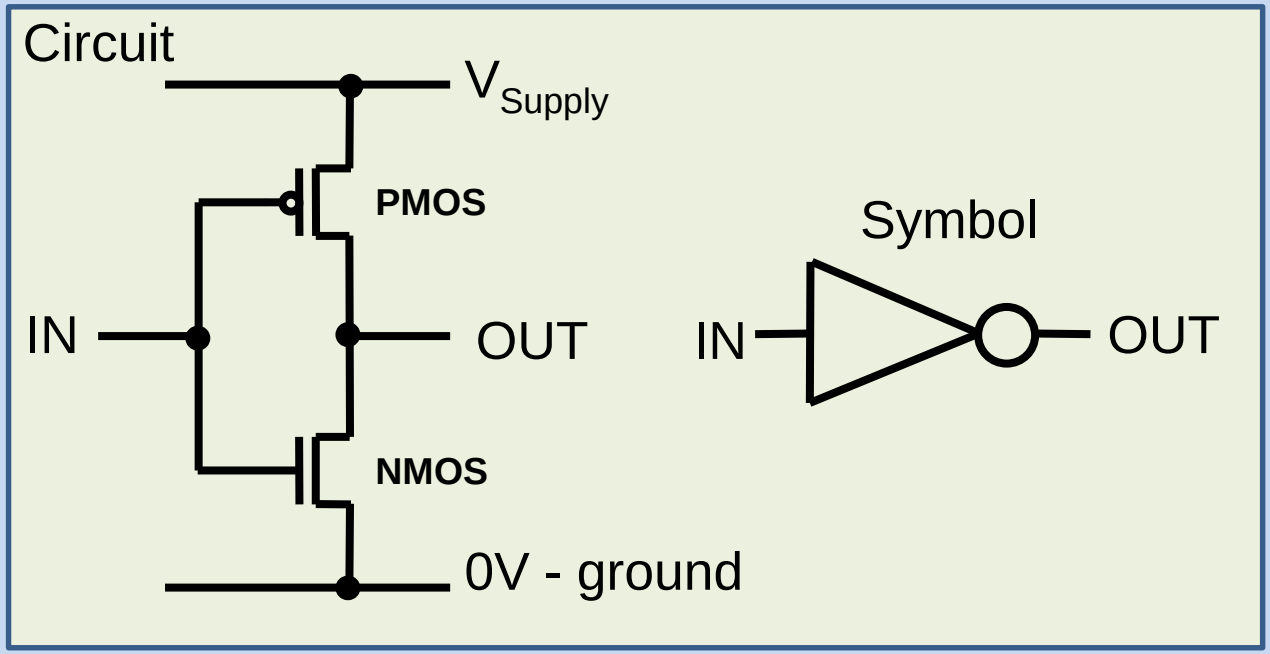
MOSFET Circuit Symbols

	Full Symbol	Full Symbol (bulk connected to source)	Simplified Symbol	Logic Symbol
P				
N				

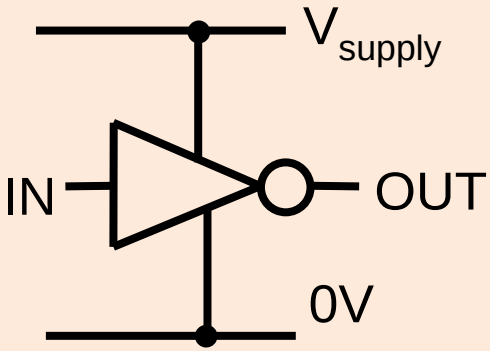
Logic symbols for the MOSFET show logic level for switch ON

- Logic 0 for the P channel device
- Logic 1 for the N channel device

The CMOS NOT gate (Inverter)



Logic gates need power supply connections but these are not normally shown on schematics



Input Logic 0

- **PMOS transistor ON** – output connected to supply – **output is logic 1**
- NMOS transistor OFF

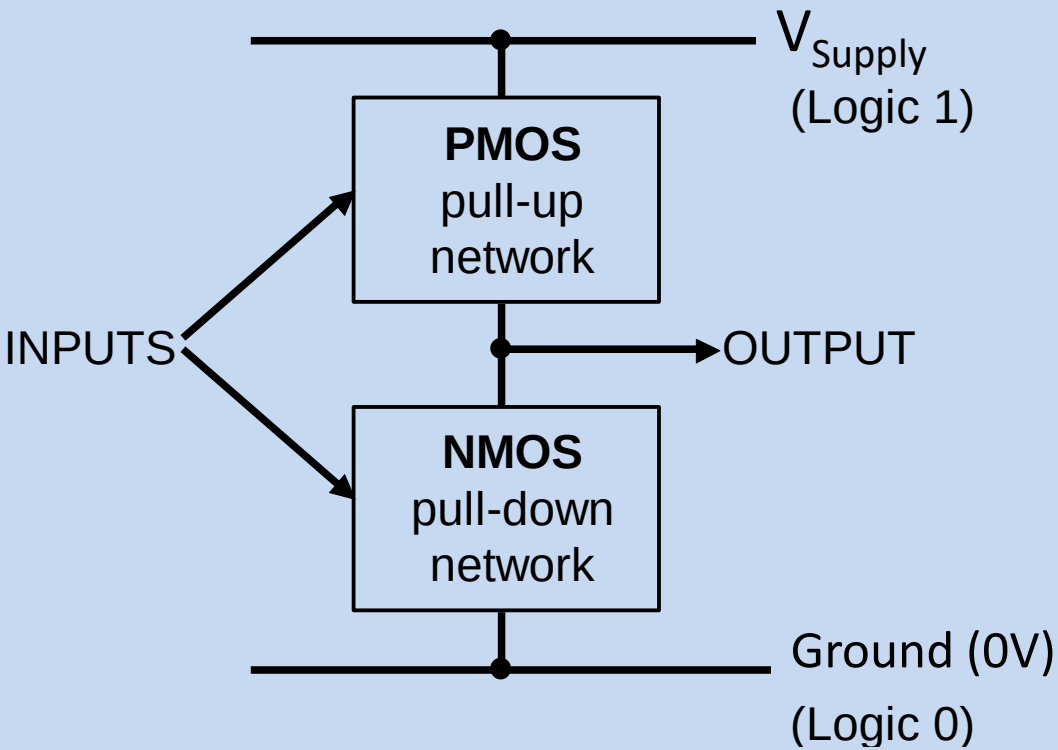
Input Logic 1

- PMOS transistor OFF
- **NMOS transistor ON** – output connected to supply – **output is logic 0**

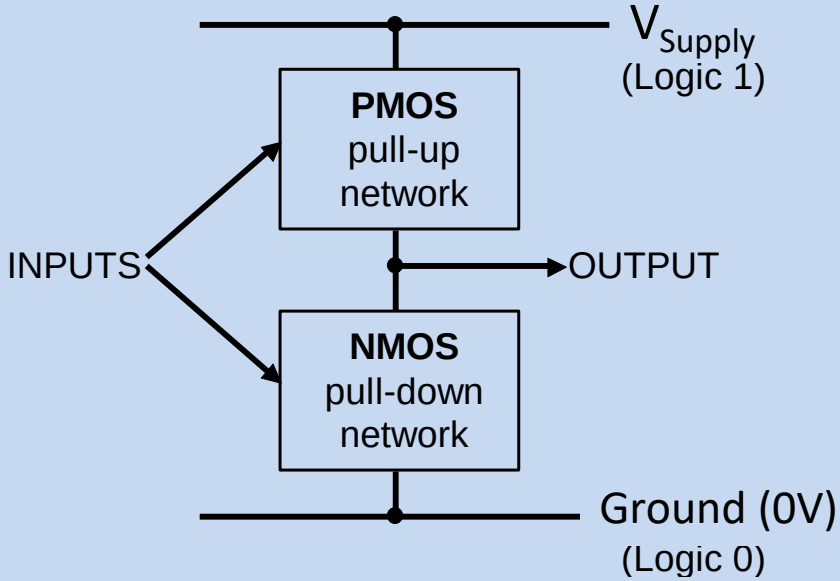
CMOS Gate Circuits

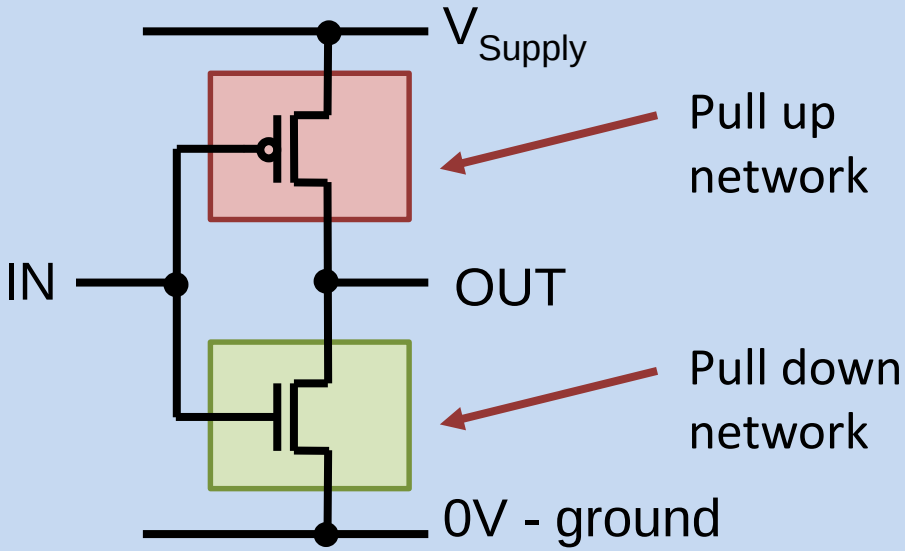
The basic form of a CMOS gate comprises a **PMOS pull-up switch network** and an **NMOS pull-down switch network**.

- The pull-up network provides a conducting path to the supply when a logic-1 output is required.
- The pull-down network provides a conducting path to ground (0V) when a logic-0 output is required.
- The networks are also referred to and ***n-blocks*** and ***p-blocks***, or more generally as ***evaluation blocks***.



The CMOS NOT gate (Inverter)





For the NOT gate the pull up and pull down networks contain one switch (transistor) each.

For other logic gates more switches are required

CMOS Gate Circuits

Gate are an extension of the form of the inverter

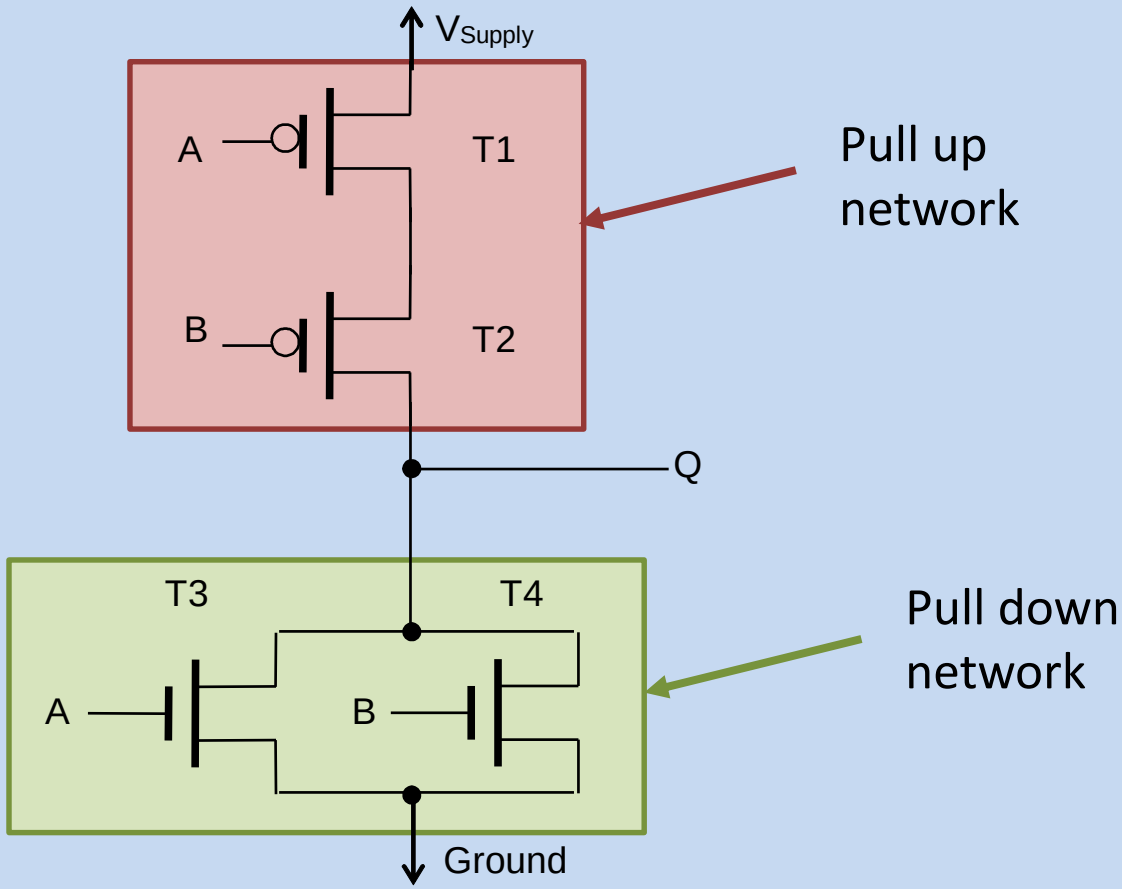
Basic gates are inverting (e.g. NAND and NOR)

An additional inverter is required for a non-inverting gates (e.g. AND)

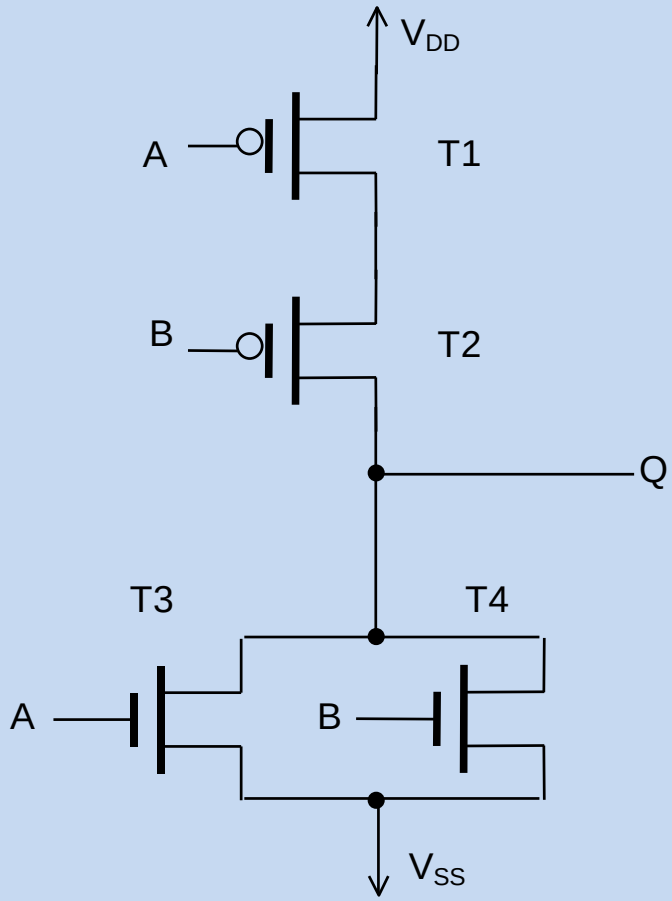
Understanding the operation of logic gates and evaluation block

- PMOS transistor: ON when its gate terminal is at logic 0
- NMOS transistor: ON when its gate terminal is at logic 1
- The P and N networks are configured to connect the output to the supply when a 1 is required and to ground when a 0 is required
- When one evaluation block is ON the other must be OFF

Example Two-Input gate



Example Two-Input gate

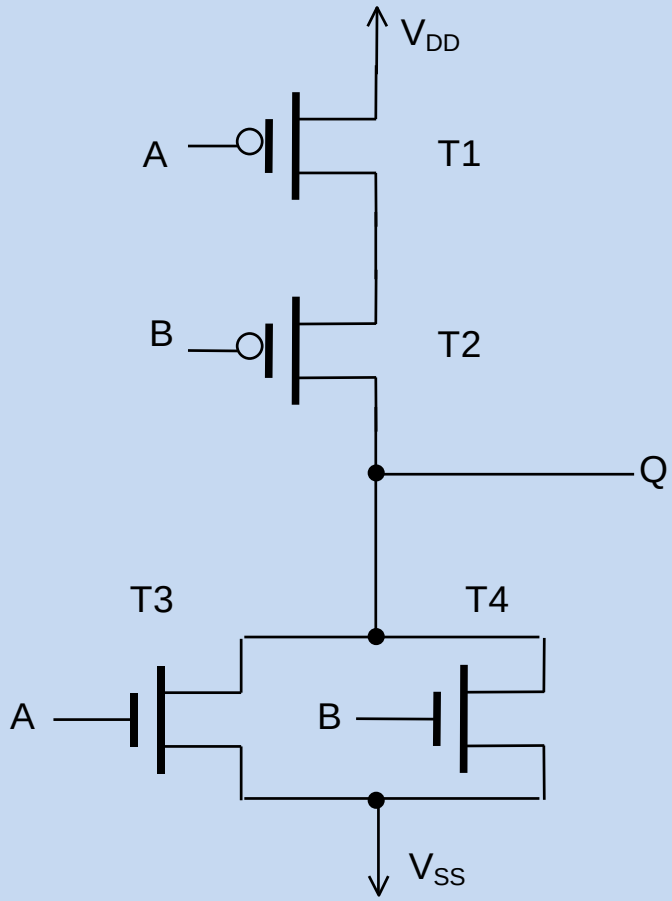


Complete the table

A	B	T1	T2	T3	T4	Q
0	0	on		off		
0	1					
1	0					
1	1					

What is the logic function?

Example Two-Input gate

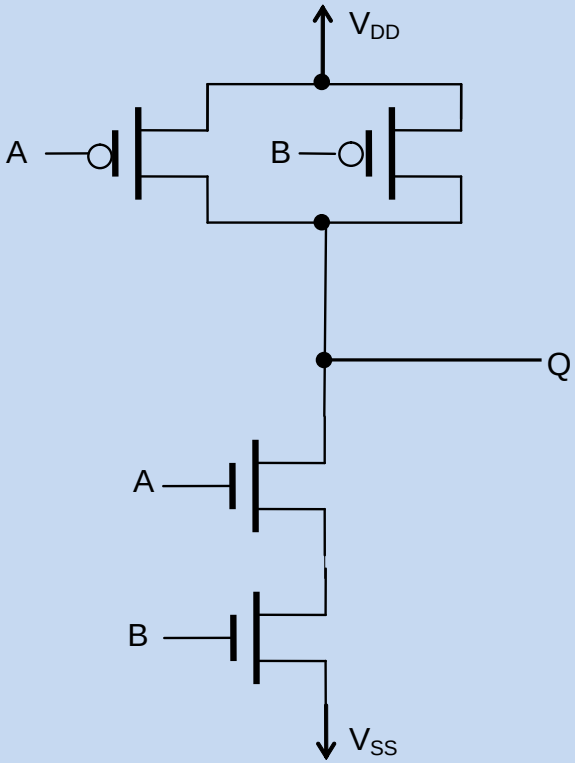


Complete the table

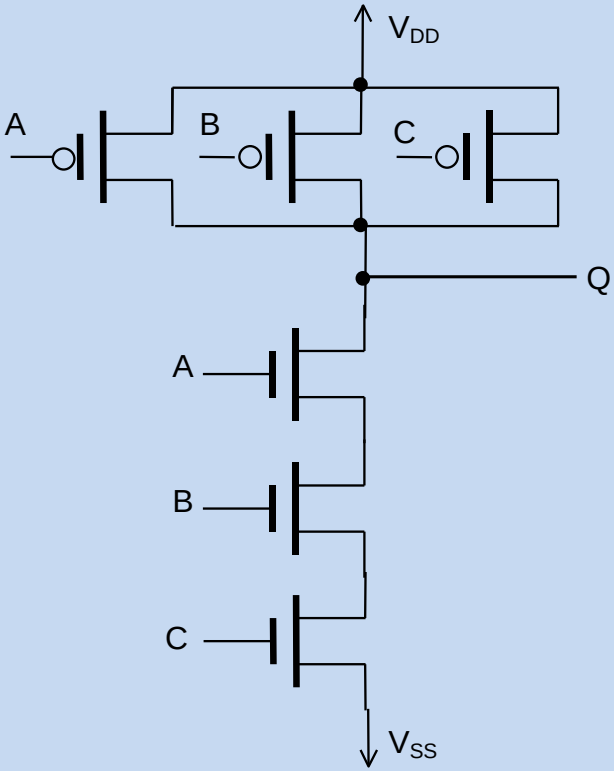
A	B	T1	T2	T3	T4	Q
0	0	on		off		
0	1					
1	0					
1	1					

What is the logic function?

Example CMOS Gate Circuits



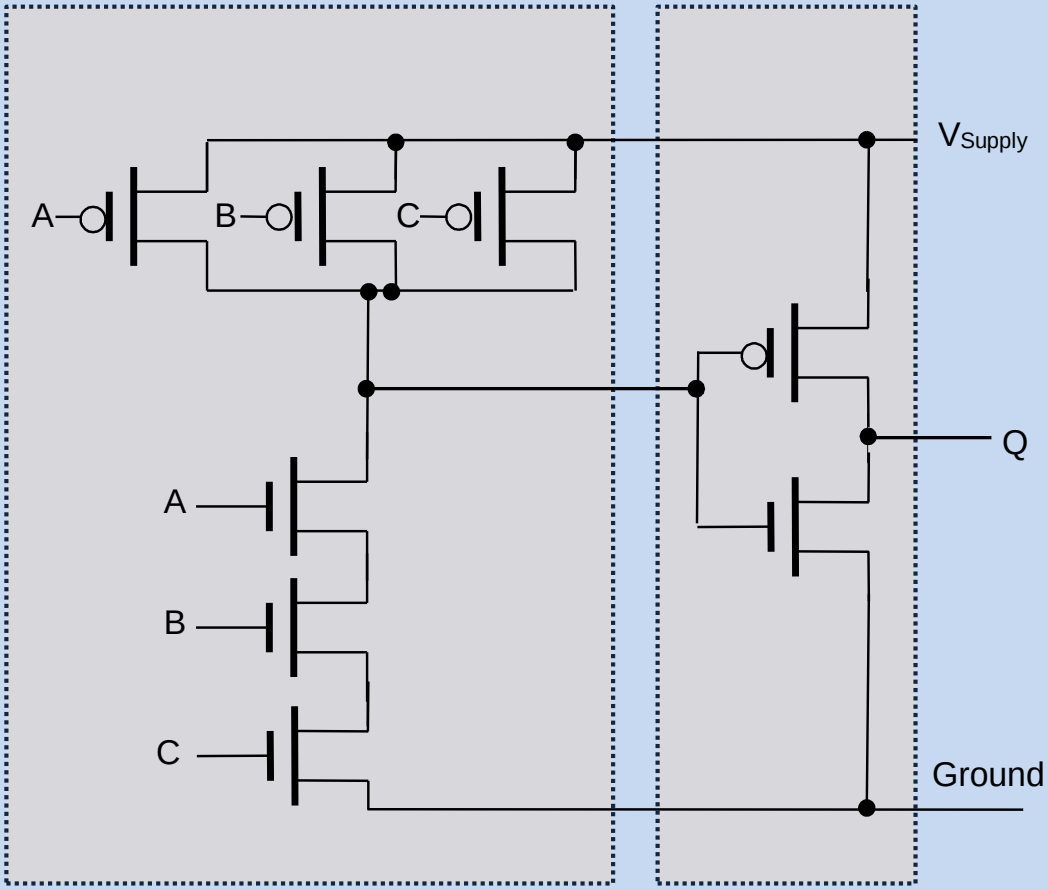
2-Input NAND

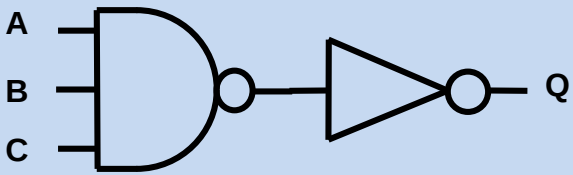


3-Input NAND

Non-inverting CMOS Logic Gates

Non inverting gates (AND and OR) are formed from the corresponding inverting gate (NAND and NOR) plus an inverter (NOT gate)





3-Input AND

Complex Gates

CMOS logic gates circuits may be devised to evaluate combinational logic functions directly (as a transistor circuit), rather than using a network of basic gates (NAND, NOR, and NOT).

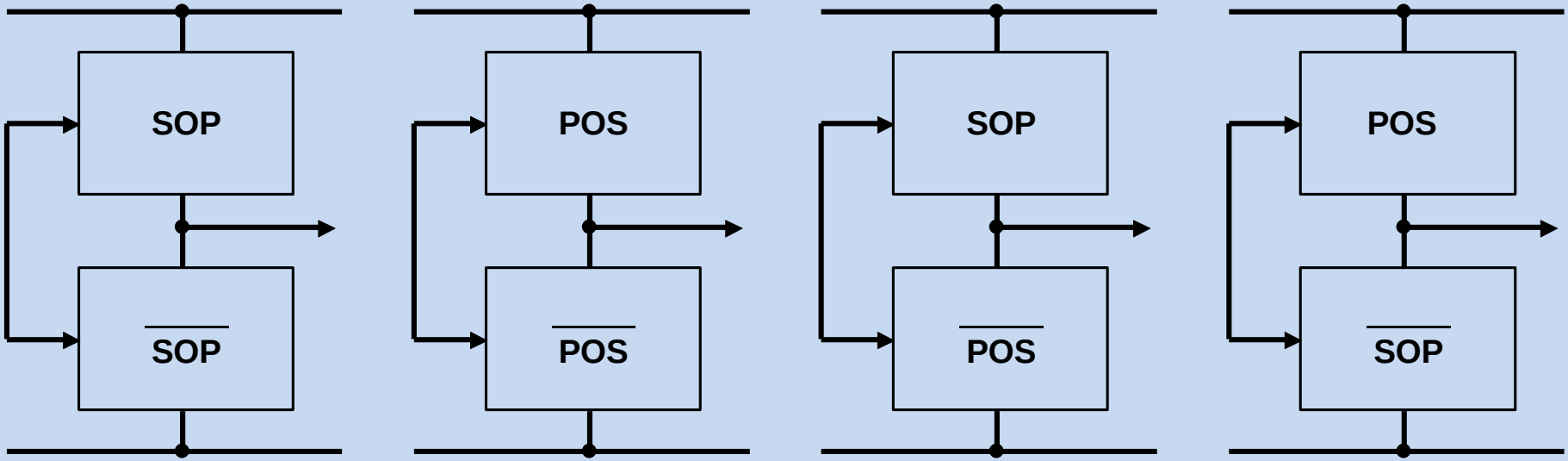
For example, function such as the following can be implemented directly with transistor switches

$$Q = \overline{AB + C} = \left(\overline{A} + \overline{B}\right) \cdot \overline{C}$$

Gates like this are sometimes referred to as *complex gates*.

Complex Gates

- In complex gates the pull-up and pull-down networks may be realised using both Sum Of Products (**SOP**) and Product Of Sums (**POS**) networks and their complements.
- This leads to a number of possible versions of some complex gates.
- Note that the NMOS network always implements the complement of the logic function because its job is to produce a 0 at the output and logic function defines the condition for an output being 1



Complex Gate Example

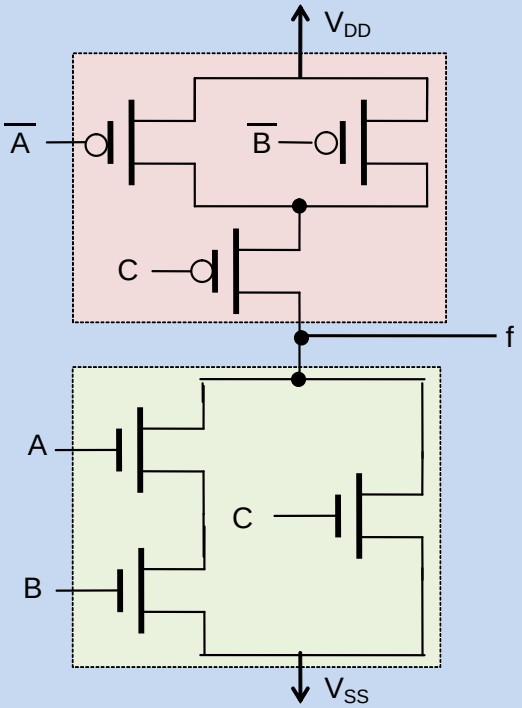
$$f = \overline{AB + C}$$

C AB	00	01	11	10
0	1	1	0	1
1	0	0	0	0

SOP $\quad f = \overline{A}\,\overline{C} + \overline{B}\,\overline{C}$

$\overline{\text{SOP}}$ $\quad \overline{f} = (A + C)(B + C)$

POS $\quad f = \left(\overline{A} + \overline{B}\right)\overline{C}$

$\overline{\text{POS}}$ $\quad \overline{f} = AB + C$

EXAMPLE $\text{POS} / \overline{\text{POS}}$